

SYSTEM MANAGEMENT

Description

The programmable SH3003 MicroBuddy® (μBuddy®) provides all mandatory microcontroller support functions:

- ◆ CPU Supervisor
- ◆ Clock Management System
- ◆ Real-Time Support
- ◆ Auxiliary functions

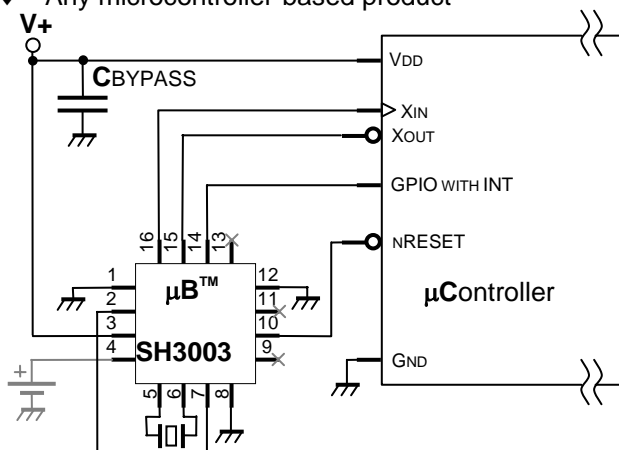
Three components make a complete system: any microcontroller, the SH3003, and a bypass capacitor. This low-cost system would consume very little power and have clock-frequency accuracy of $\pm 0.5\%$. A fourth component, a 32.768 kHz crystal, raises the clock frequency accuracy to $\pm 0.0256\%$ (± 256 ppm).

The SH3003 can operate completely stand-alone, or under control of the microcontroller. A single-wire interface handles both bi-directional communications and the interrupt / wake-up signal from the SH3003. The SH3003 stores all configuration, calibration, parameters, and status information in a 36-byte bank of control registers. On reset, most of these are reloaded with defaults from the factory-set nonvolatile memory. The microcontroller can change any settings on the fly. If some of the settings must remain fixed, a comprehensive set of write-protect bits is provided for several related groups of registers (with both permanent write-inhibit and lock/unlock capabilities).

A backup power source may also be connected to the SH3003. The IC can directly accommodate 2/3-cell zinc-carbon/alkaline, 2/3-cell mercury, 2/3/4-cell NiCd/NiMH, 1-cell Li/Li+ batteries, or a super cap.

Applications

- ◆ Home automation and security
- ◆ Consumer products
- ◆ Portable/handheld computers
- ◆ Industrial equipment
- ◆ Any microcontroller-based product

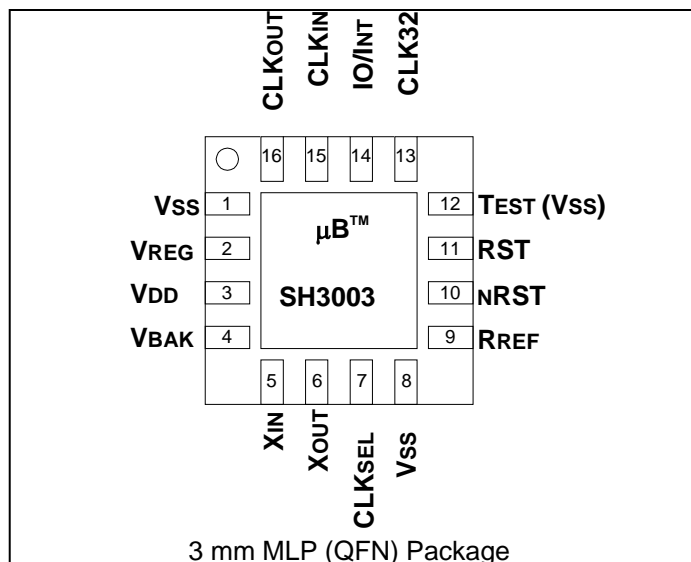


Typical Application Circuit with High Clock Accuracy

Features

- ◆ **Highly integrated IC**
 - 3 mm x 3 mm x 0.9 mm 16-lead MLP (QFN) package
- ◆ **CPU Supervisor**
 - Low VDD reset programmable from 2.3 V to 4.3 V
 - Watchdog timer with programmable timeout periods
 - Both active-high and active-low reset outputs
- ◆ **Clock Management System**
 - Replaces high-frequency (HF) crystal or resonator
 - Programmable clock output from 32.768 kHz to 16 MHz
 - Speed shift between multiple clock frequencies
 - Adjustable spectrum spreading for EMI reduction
 - Directly supports microcontroller STOP function
 - Deep sleep with instantaneous auto-wakeup
- ◆ **Real-Time Support**
 - 179-year real-time clock, battery-backup capable
 - Dedicated 32.768 kHz buffered clock output
 - Built-in trim for 32.768 kHz oscillator to ± 4 ppm
 - Programmable periodic interrupt / wakeup timer
- ◆ **Auxiliary functions**
 - 4-byte (32-bit) scratchpad RAM, loaded on reset with factory-set value (zero or optional ID code)
 - All settings programmable in real time, defaults restored from nonvolatile memory on reset
- ◆ **Operates from 2.3 V to 5.5 V**
- ◆ **IDD < 850 μ A / 2 MHz, < 3 mA / 16 MHz, < 10 μ A/standby**
- ◆ **IBUP < 2 μ A / IBSB < 50 nA (battery backup / standby)**

Pin Configuration



Semtech, the Semtech logo, MicroBuddy, μBuddy, and μB are marks of Semtech Corporation. All other marks belong to their respective owners.

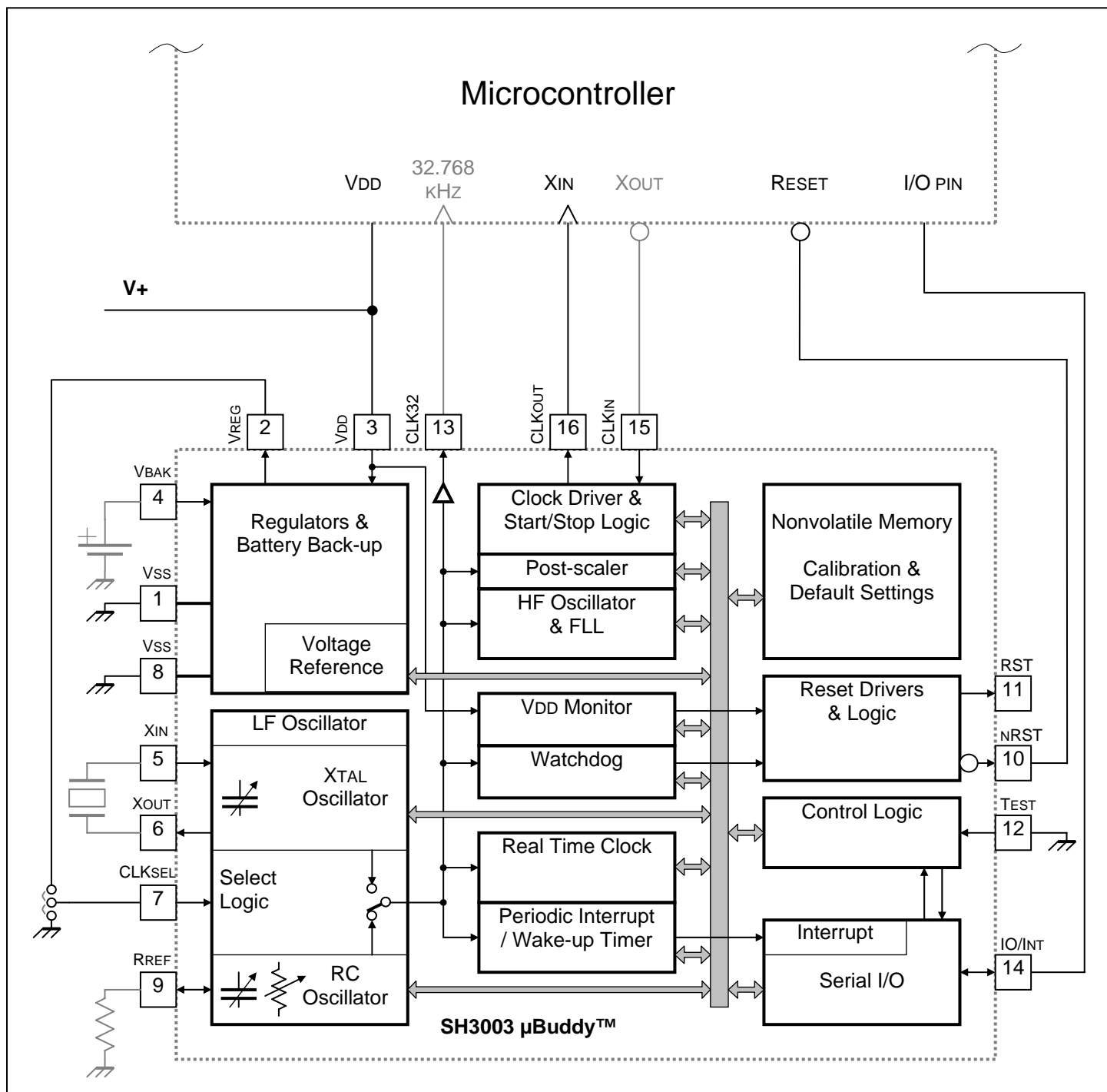
SYSTEM MANAGEMENT

Description

Ordering Information

SH3003IMLTR	IC	MLP 3 x 3 mm, 16 pins, temp. range -40° C to +85° C
EVK-SH3000USB	SH3000 evaluation kit	
SH3000EK.pdf	SH3000 Evaluation Kit User Guide	
SH3000UM.pdf	SH3000 Reference Manual	

Block Diagram



SYSTEM MANAGEMENT
Pin Descriptions

Pin	Name	Type	Function
—			Thermal pad – connect to ground
1	VSS	Power	Ground, 0 V. All VSS pins and TEST (VSS) pin must be connected together.
2	VREG	Power	Output of internal Voltage Regulator, 2.2 V nominal. This pin can power external loads of <5 mA. If load is “noisy” it requires a bypass capacitor. May be left unconnected or used as a high logic level signal for CLKSEL pin (see below).
3	VDD	Power	Main power supply, +2.3 to +5.5 V.
4	VBAK	Power	Backup power supply for real-time clock, +2.3 to +5.5 V (+1.8 to +5.5 V typical). This voltage can be higher or lower than VDD. Connect a backup battery or backup capacitor (with external recharge circuit). Connect to VDD if not used.
5	XIN	Analog In	Oscillator pins for optional external low frequency crystal, typically 32.768 kHz crystal with nominal 12.5 pF load capacitance. Keep open or connect to Vss if not used.
6	XOUT	Analog Out	
7	CLKSEL	Digital In	A logic low level selects the internal 32.768 kHz RC oscillator (CLKSEL tied to Vss). A high state on this pin selects the 32.768 kHz crystal oscillator (CLKSEL is connected to VREG). The SH3003 always starts up using the internal 32.768 kHz RC oscillator. If CLKSEL is high, the internal 32.768 kHz clock switches to the crystal oscillator once it has stabilized, and RC oscillator is disabled for power conservation. Do not connect CLKSEL to any signals except VSS or VREG. CLKSEL must not be left open.
8	VSS	Power	Ground, 0 V. All VSS pins and TEST (VSS) pin must be connected together.
9	RREF	Analog	Optional 1 MOhm external bias resistor for the internal 32.768 kHz RC oscillator. Can be used to set, trim or modulate the internal RC oscillator. Keep open if not used.
10	NRST	Digital Out	Active low system reset output. Asserted with a strong low state when a reset condition occurs. Weakly pulled to VDD internally when not active. This signal is valid for VDD as low as 1 V. Keep open if not used.
11	RST	Digital Out	Active high system reset output. Asserted with a strong high state when a reset condition occurs. Weakly pulled to VSS internally when not active. This signal is valid for VDD as low as 1 V. Keep open if not used.
12	TEST (VSS)	Digital In	Factory test enable. All VSS pins and TEST (VSS) pin must be connected together.
13	CLK32	Digital Out	Buffered internal 32.768 kHz clock, derived according to the CLKSEL pin setting. This pin uses backup power for the buffer when VDD is not present. When driving high, this signal is either at VBAK or VDD (if VDD is higher than the reset threshold). When enabled, this signal runs continuously independent of CLKOUT activity. Minimize the external load to reduce power consumption during backup operations. When disabled, this pin is driven to Vss. Keep open if not used.
14	IO/INT	I/O	Serial communications interface and interrupt output pin. This pin is internally weakly pulled to the opposite of the programmed interrupt polarity. For example, if interrupt is programmed to be active low, this pin is weakly pulled to VDD when inactive. Keep open if not used.
15	CLKIN	Digital In	Clock activity sense input. Used to detect when the target microcontroller enters stop mode (which disables its clock). Connect to the microcontroller's clock output or oscillator output pin. Connect to Vss when not used. CLKIN must not be left open.
16	CLKOUT	Digital Out	Programmable high frequency clock output. Connect to the target microcontroller's clock input or oscillator input pin. Keep open if not used.

SYSTEM MANAGEMENT**Functional Description**

The SH3003 is a single-chip support system for microcontrollers, microprocessors, DSPs and ASICs. It consists of four major functional blocks, each block having numerous enhancements over alternative solutions.

The major modules are the CPU Supervisor, the Clock Management System, the Real-Time Support, and the Auxiliary functions.

The entire chip is controlled by the set of internal registers and accessed via the single-pin serial interface. All of the settings, configuration, and calibration or operating parameters are programmable and re-programmable at any time. All of the parameters required for stand-alone operations are initialized on reset from the built-in factory-programmed nonvolatile memory. This allows the SH3003 to operate autonomously for most of its supervisory functions. The stand-alone operations do not require the use of the serial interface or any of the initialization and control operation, but without these, the full potential benefit of the SH3003 may not be realized.

In the preferred configuration, where the SH3003 is tightly coupled to the target micro, the SH3003 offers an unprecedented level of design flexibility in clock and power usage management.

The SH3003 is a particularly desirable integration because the built-in features interact and meld to produce more useful system level functions.

For example, on power up, the SH3003 can quickly release the reset lines on its CPU Supervisor module because the clock signal from the Clock Management System is guaranteed to be running and stabilized. An ordinary reset circuit must hold reset active for a long time to allow an unknown crystal to start up and stabilize.

The SH3003 offers several ways to minimize system power consumption, such as allowing the target processor to enter deep sleep by stopping its clock completely, and to wake up as often as necessary with no external support. The clock can be programmed to start up at a given frequency, and software can adjust it dynamically to manage power consumption and different operating modes.

Users should consider the interactions of the major functional blocks to gain the maximum advantage from the SH3003.

The individual functional blocks are described in the following sections.

Default Start-Up Parameters

While the operating parameters of the SH3003 are programmable by the host microcontroller at any time, the default start-up parameters and appropriate calibration values are programmed into the chip's nonvolatile memory at the factory. This enables the SH3003 to be used stand-alone or in an embedded application with minimal microprocessor intervention.

Default Start-Up Parameters for the SH3003 are

- Reset and VBO voltage level is 2.3V
- CLKOUT frequency is 16.0 MHz
- CLK32 output is disabled
- Spread spectrum is disabled
- Internal RC oscillator is calibrated (to nominal frequency of 32768 Hz)

Internal load capacitors on the 32.768 kHz crystal oscillator pins are set to 12.5 pF

SYSTEM MANAGEMENT

CPU Supervisor

The SH3003 has two supervisory functions that manage the reset of the target processor, a low VDD monitor (Brownout Detector) and a Watchdog Timer, see **Figure 1**.

Both functions are integrated with the Clock Management System to provide a more complete system solution than stand-alone components.

The SH3003 has both active high and active low reset output pins. Both are driven strong to the active state and weak to the inactive state. This eliminates the need for external pull-ups and allows various reset sources to be connected together in a wire-OR configuration. (This makes it simple to set up a manual reset circuit.)

A set of flags in the register map indicates the source of the reset to the system software.

Low VDD Reset

The SH3003 drives the reset pins active whenever VDD is below the value of VBO, the brownout reset threshold, programmable from 2.3 V to 4.3 V in average steps of 33 mV, see **Table 1**.

Table 1. Programmable VBO Values

Parameter	Min	Typ	Max	Units
VBO for min code (000000)	2.27	2.3	2.33	V
VBO for max code (111111)	4.2	4.3	4.4	V
Step resolution		33		mV

The default VBO value is loaded on power-up from the factory-programmed nonvolatile memory. It can be re-programmed at any time or it can be permanently protected from any changes by setting the VBO Lock flag or a write-protect flag.

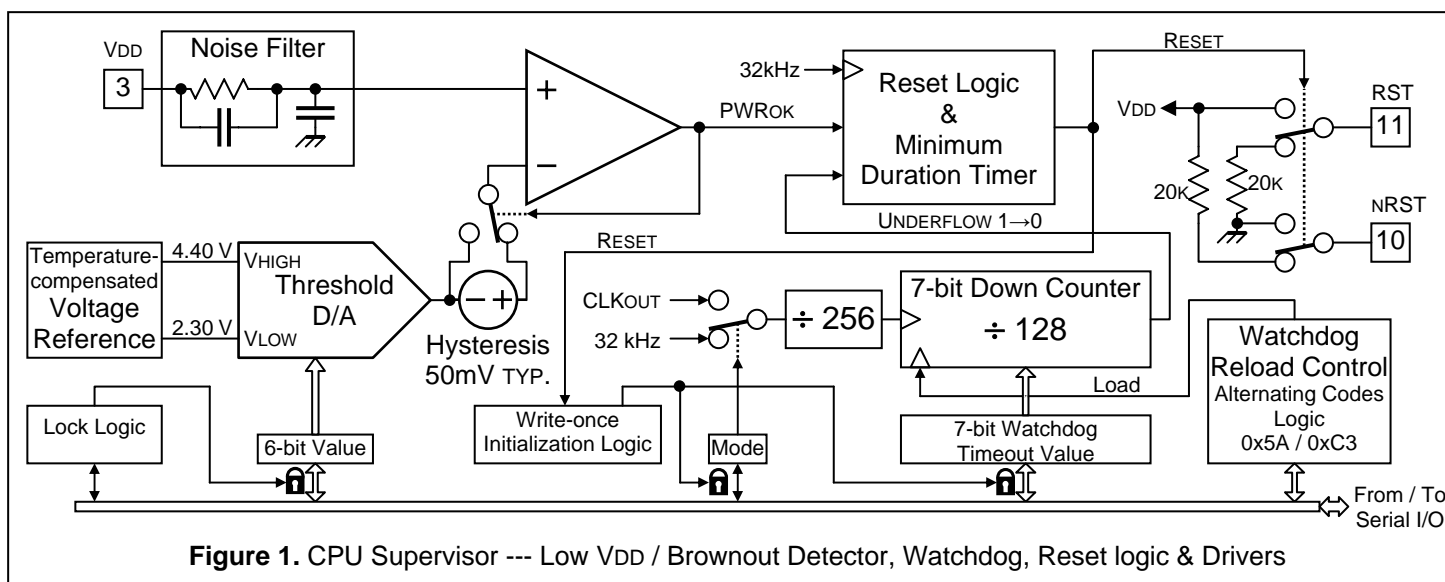
On power up both the active-high and active-low reset signals are driven active. These outputs are typically valid for a VDD level of at least 0.5 V, and guaranteed to be valid for a VDD level of 1.0 V.

The reset outputs remain active until VDD rises and stays above the level of (VBO + VHYST), where VHYST is a small fixed amount of hysteresis, nominally 50 mV, added to prevent nuisance reset activations (when VDD slowly changes near the level of VBO and some noise or power glitching is present).

At the level of (VBO + VHYST) the power supply is considered valid. In case of the initial power-up, the reset is then driven inactive once 6 ms of valid power have elapsed. In the case of brownout, the reset is released after a delay of 6 ms (but no less than 12 ms from the beginning of the brownout).

Such a fast reset is possible because the SH3003 provides a fast-starting clock that is free of crystal start-up time requirements. This gives the SH3003 an advantage over most external reset circuits, which must have a long reset pulse duration to accommodate long and unpredictable crystal start-up times.

The SH3003 guarantees that a valid and stable clock is available 2 ms before the reset signals are negated, so that internal synchronous reset and initialization of the target micro can proceed normally.



SYSTEM MANAGEMENT

Since the clock is only active for the last 1 or 2 ms of the reset interval, when VDD has already been valid for some time, energy savings are realized and the startup of the whole system is made easier. The commonly used reset approach forces the processor to turn the oscillator on and to run at full speed (thus consuming full power) during the critical time when the (possibly depleted) battery is trying to raise VDD to an acceptable level. In contrast, the SH3003 allows the power source to charge the bypass capacitors and raise the level of VDD with little additional load. Only when power has stabilized is the target micro permitted to start expending energy.

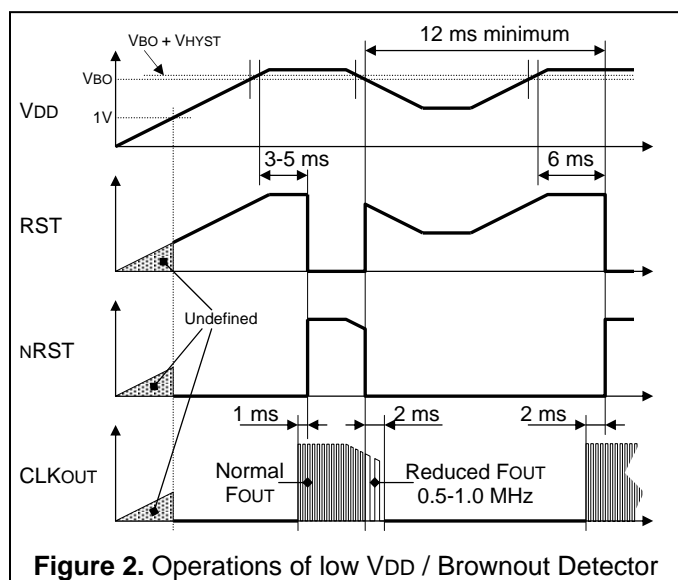
When a brownout event occurs, the SH3003 continues to provide the clock to the target processor, but at a reduced frequency between 500 kHz and 1.0 MHz. After a delay of 2 ms this clock is stopped, automatically lowering the energy consumption of the whole system, see **Figure 2**.

A Noise Filter (see **Figure 1**) prevents reset activations from noise and small power glitches on the VDD line. A typical behavior is shown in **Figure 3** for the VDD level just above VBO and various amplitudes and durations of the negative-going spikes.

When VDD is falling, both reset lines are guaranteed to activate within 5 μ s from the time VBO is crossed over.

Watchdog Timer

The second circuit for supervising the processor is the watchdog timer. Whereas the low VDD / Brownout Detector monitors supply voltage, the watchdog timer monitors behavior. It is based on a programmable timer that must be restarted periodically by the host micro. If software fails to restart the timer, the watchdog resets the processor.



Restarting the timer takes considerable processing, making it unlikely that it would occur accidentally, as might happen for a simple pin-strobe configuration of a typical watchdog IC.

The watchdog is disabled after reset occurs. It stays disabled until initialized by the host processor.

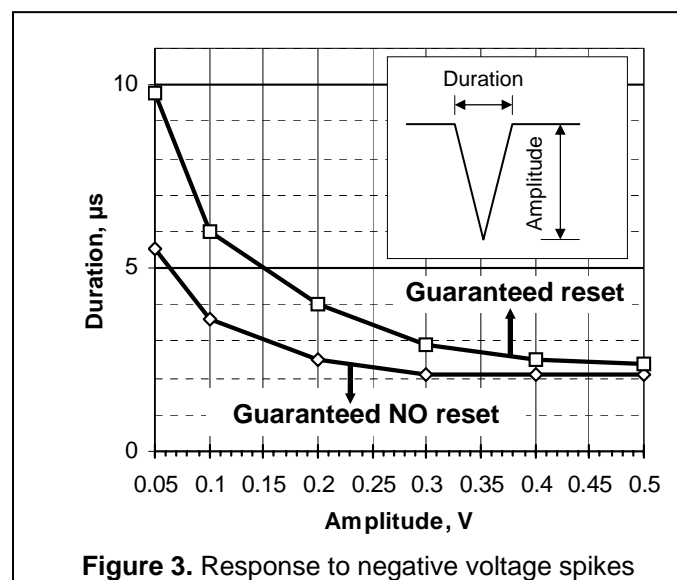
The initialization requires the watchdog clock mode to be selected (see **Figure 1**) and the 7-bit time-out value to be set. As soon as the time-out is written, the watchdog begins operations and can not be stopped; also, the time-out value and or clock source can no longer be changed.

The two clock sources available for the watchdog are the internal 32.768 kHz clock and the CLKOUT signal.

When operating from the 32.768 kHz source, the time-out interval is programmable from 7.8125 ms to 1 second with resolution of 7.8125 ms. The internal 32.768 kHz clock is running all the time, therefore the time-out duration is fixed and predictable.

When operating from the CLKOUT signal the time-out interval is programmable between 256 and 32768 cycles of CLKOUT with resolution of 256 cycles. The actual time-out duration is variable and depends both on the frequency of CLKOUT signal and the amount of time the target micro spends in the STOP mode, when the CLKOUT signal is also stopped.

These two clock modes, together with the programmable time-out value, allow the SH3003 exceptional flexibility, previously unattainable by existing discrete watchdog solutions.



SYSTEM MANAGEMENT

The watchdog timer is kept from timing out by periodic reload of the time-out value, triggered by a write of a code byte to the Watchdog Reload Register. As a further safety measure, there are two different and alternating code bytes that should be written to the same Watchdog Reload Register. The code values are 0x5A and 0xC3. The timer is reloaded after every write of a single code byte.

The code byte should be written to the Watchdog Reload Register, or reset is activated when the watchdog timer expires. Also, reset is initiated immediately if the value of the code byte is incorrect or out of sequence. When the watchdog triggers the reset, its duration is 12 ms.

Using two separate software routines, each to write one of the code values, results in the highest level of system security. These routines must execute in the correct order. It is unlikely that runaway code could manage this. In addition, this design makes it difficult for the code to become stuck in a tight loop resetting the watchdog.

Clock Management System

The SH3003 provides a flexible tool for creating and managing clocks, a versatile and accurate “any frequency” clock synthesizer (see **Figure 4**).

It is capable of generating any frequency in the range of 62.5 kHz to 16.0 MHz, with worst-case resolution of 0.0256% (256 ppm). The internal 32.768 kHz clock can also be routed to the CLKOUT pin (and HF oscillator stopped for energy savings).

The objectives, features, and behavior of the Clock Management System are aimed towards the systems that utilize a microcontroller, a microprocessor, a DSP or an ASIC.

The SH3003 permits the automatic sensing of the intentions of the host processor, an industry first. The SH3003 shuts down its clock output when it senses that the host processor issued a STOP instruction. Subsequently, the SH3003 idles, consuming less than 10 μ A. As soon as the host exits the STOP mode, the SH3003 instantaneously starts to supply a stable clock (<2 μ s wake-up).

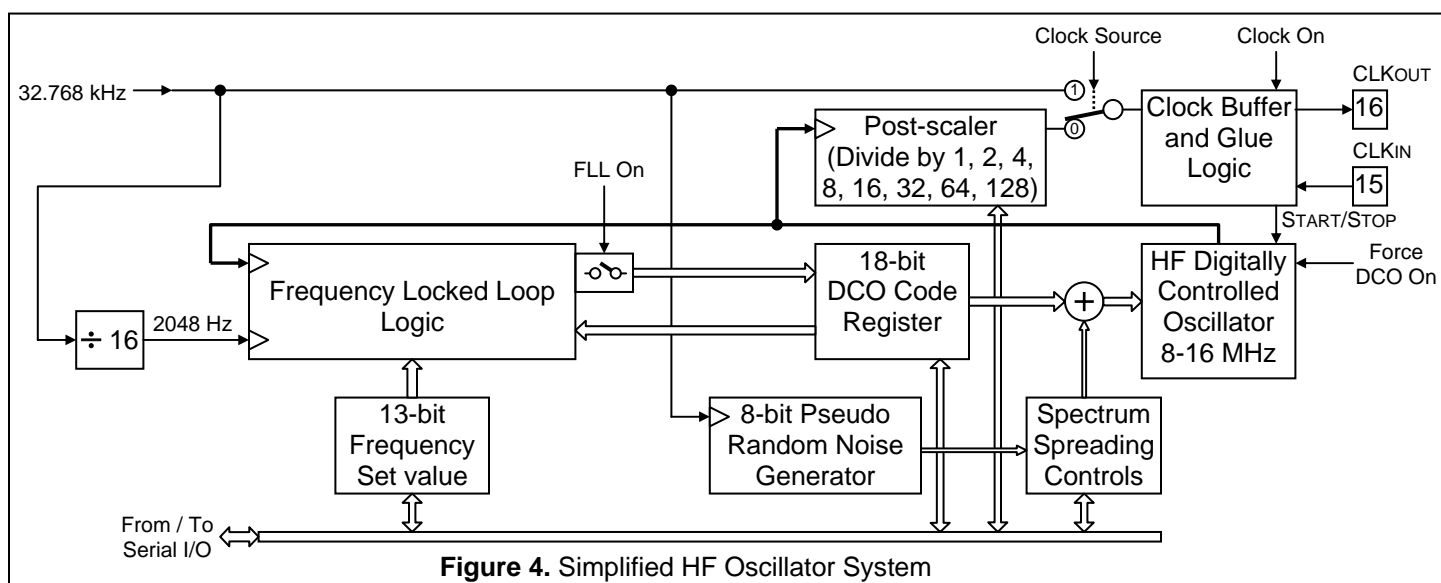
A typical system, constructed with a ceramic resonator or a crystal as the frequency determining element, must wait at least several hundred microseconds (for a resonator), or as much as 100 ms or more (for a HF crystal), to re-start the oscillator. The SH3003 allows the response to and service of an event to finish with a speed previously unattainable for a simple microprocessor. A system with a traditional clock approach may be as much as 100x – 10,000x slower.

Clock Generator Operation

The frequency synthesizer in the SH3003 is constructed from the 2:1 tunable 8.0 –16.0 MHz HF oscillator followed by a programmable “power-of-two” post-divider (see **Figure 4**).

The Clock Source selector and the programmable post-scale divider allow instantaneous switching between the 32.768 kHz internal clock and divided-down HF oscillator output. There is no settling or instability when the switch occurs.

This is a preferred method for clock control in computing systems, when the large ratio between high and low frequency of operations allows for correspondingly large and instantaneous savings in power consumption.



SYSTEM MANAGEMENT

When the HF oscillator is operating alone, it can set the frequency of the clock on the CLKOUT pin to $\pm 0.025\%$, and maintain it to $\pm 0.5\%$ over temperature. This compares favorably with the typical $\pm 0.5\%$ initial clock accuracy and $\pm 0.6\%$ overall temperature stability of ceramic resonators. The SH3003 replaces the typical resonator, using less space and providing better performance and functionality.

The HF oscillator can also be locked to the internal 32.768 kHz signal. The absolute accuracy and stability of the HF clock depends on the quality of the 32.768 kHz internally generated clock; the low-frequency (LF) Oscillator System is described later in this document.

When the Real-Time Clock module of the SH3003 is used for high-accuracy timekeeping, an external 32.768 kHz crystal used as a reference for RTC provides excellent accuracy and stability for the Clock Management System.

The SH3003 employs a Frequency Locked Loop (FLL) to synchronize the HF clock to the 32.768 kHz reference. This architecture has several advantages over the common PLL (Phase Locked Loop) systems, including the ability to stop and re-start without frequency transients or instability, and with instant settling to a correct frequency. The conventional PLL approach invariably includes a Low-Pass Filter that requires a long settling time on re-start.

The primary purpose of the FLL is the maintenance of the correct frequency while the ambient temperature is changing. As the temperature drift of the HF oscillator is quite small, any corrective action from the FLL system is also small and gradual, commensurate with the temperature variation.

The FLL system in the SH3003 is unconditionally stable.

To set a new frequency for the FLL, the host processor writes the 13-bit Frequency Set value. The resulting output frequency is calculated using simple formulas [1] and [2] (reference frequency is 32.768 kHz):

$$F_{osc} = 2048 \text{ Hz} * (\text{Frequency Set value} + 1) \quad [1]$$

$$F_{out} = F_{osc} / (\text{Post-divider setting}) \quad [2]$$

For example, a post-divider setting of $\div 8$ and the Frequency Set value of 4000 (0x0FA0) produce an output frequency of 1.024 MHz.

SYSTEM MANAGEMENT
Programmable Spectrum Spreading

Most commercial electronic systems must pass regulatory tests in order to determine the degree of their Electromagnetic Interference (EMI) affecting other electronic devices. In some cases compliance with the EMI standards is costly and complicated.

The SH3003 offers a technique for reducing the EMI. It can be a part of the initial design strategy, or it can be applied in the prototype stage to fix problems identified during compliance testing. This feature of the SH3003 may greatly reduce the requirements for radiofrequency shielding, and permits the use of simple plastic casings in place of expensive RFI-coated or metal casings.

The SH3003 employs Programmable Spectrum Spreading in order to reduce the RF emissions from the processor's clock. There are five (5) possible settings; please see **Table 2** for operating and performance figures in the 8–16 MHz range.

Table 2. EMI reduction with Spectrum Spreading

Setting			Spreading Bandwidth kHz	Peak EMI Reduction (guaranteed) db	Peak EMI Reduction (measured) db
En	CFG1	CFG0			
0	X	X	Off	0	0
1	0	0	32	-3	-3
1	0	1	64	-6	-7
1	1	0	128	-9	-10
1	1	1	256	-12	-15

Spectrum Spreading is created by varying the frequency of the HF oscillator with a pseudo-random sequence (with a zero-average DC component). The Maximum-Length Sequence (MLS) 8-bit random number generator, clocked by 32.768 kHz, is used. Only 4, 5, 6, or 7 bits of the generated 8-bit random number are used, according to the configuration setting.

Maximum fluctuations of the frequency depend on the selected frequency range and the position within the range. Selecting the HF oscillator frequency to be near the high end of the range limits the peak variations to $\pm 0.1\%$, $\pm 0.2\%$, $\pm 0.4\%$, or $\pm 0.8\%$ (corresponding to the configuration setting).

Special Operating Modes

The SH3003 can operate stand-alone, without connections to the In and Out terminals of the host's oscillator. For example, a bank of SH3003 chips can generate several different frequencies for simultaneous use in the system, all controlled by a single micro (and possibly sharing one 32.768 kHz crystal by chaining the CLK32 pin to XIN pin on the next device). In this case the CLKIN pin should be connected to Vss. The clock output on the CLKOUT pin is continuous; the correct operating mode is automatically recognized by the SH3003.

A microcontroller may not have a STOP command. With the SH3003, this controller can do a "simulated" STOP by issuing an instruction to the SH3003 to stop the clock. This command is accepted only if the Periodic Interrupt / Wakeup Timer has started (otherwise, once the system is put to sleep, it would never wake up again). This mode of operations is only possible if the host processor is capable of correct operations with clock frequency down to zero, and keeps all of the internal RAM alive while the clock is stopped.

SYSTEM MANAGEMENT
Real-Time Support

The SH3003 has two support modules that are specifically designed for various real time support functions. They are the Real-Time Clock and the Periodic Interrupt / Wakeup Timer. Both of these units as well as other functions of the SH3003 depend on the internal 32.768 kHz clock for accuracy.

The SH3003 allows a trade-off between the cost of a system and its accuracy.

For some devices, a single SH3003 without any support components provides sufficient accuracy. These units can operate with processor clock accuracy of $\pm 0.5\%$ and the accuracy of the real-time system of $\pm 3\%$.

At the other end of the spectrum, with one external component (a 32.768 kHz crystal), the SH3003 can provide a processor clock accuracy of ± 256 ppm ($\pm 0.0256\%$) and the accuracy of the real-time system of ± 4 ppm ($\pm 0.0004\%$).

Low Frequency (LF) Oscillator System

This module provides the 32.768 kHz clock to all internal circuits and to the dedicated output pin, CLK32.

If enabled, the CLK32 output continues normal operations when VDD is absent and backup power is available.

When the power is first applied to the SH3003, the RC oscillator takes over. It supplies the 32.768 kHz clock for start-up and initialization. However, if the CLKSEL pin is set high, then the crystal oscillator is enabled. Once the crystal has started and stabilized, the internal 32.768 kHz clock switches to the very accurate crystal frequency; see **Figure 5**.

Just like the VBO value for the Reset circuit, the default calibration values for the RC oscillator are loaded on power-up from the factory-programmed nonvolatile memory. They can be re-programmed at any time or they can be permanently protected from any changes by setting the Lock flag or a write-protect flag. Factory calibration brings the frequency of the RC oscillator within $\pm 3\%$ of the 32.768 kHz for the internal reference resistor, and $\pm 2\%$ for the external 1 M Ω 1% resistor, over the entire temperature and supply voltage range.

The frequency of the RC oscillator can be tuned or modulated by varying the external reference resistor, which should be located as close as possible to RREF, pin 9.

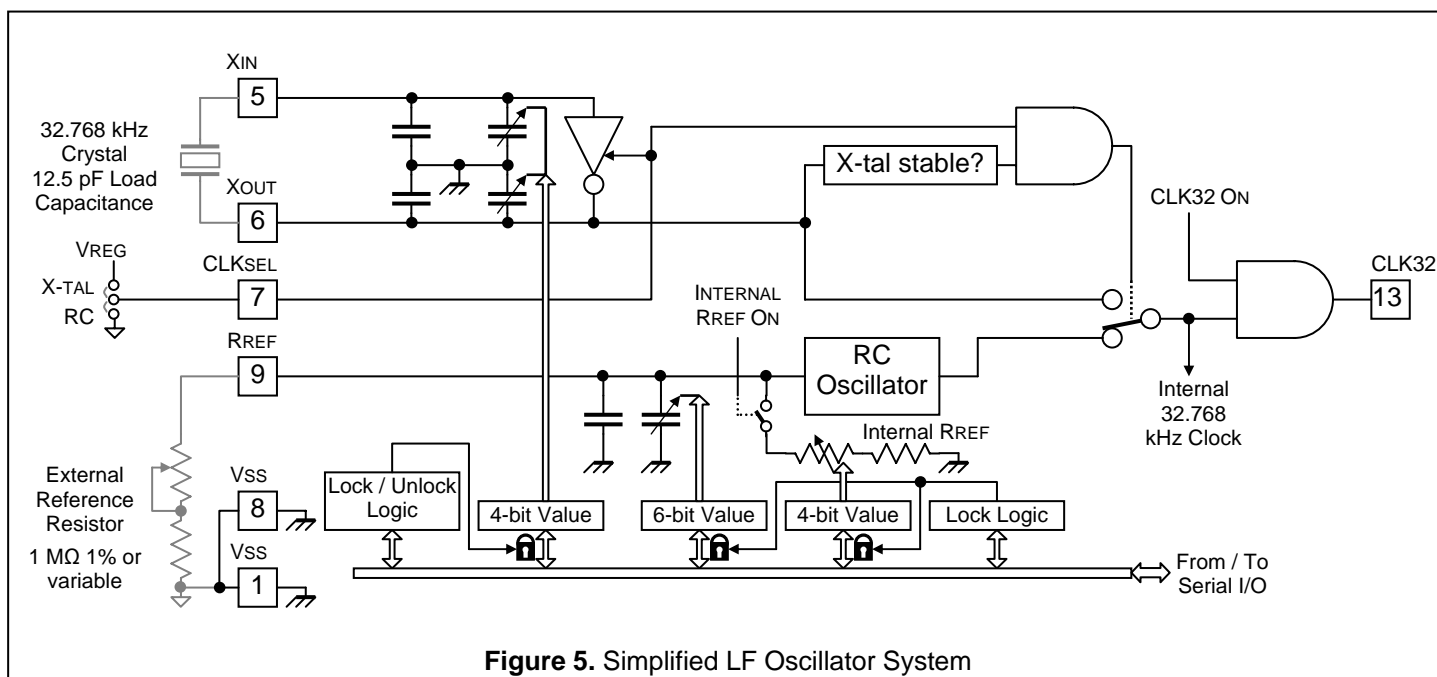


Figure 5. Simplified LF Oscillator System

The crystal oscillator has the useful feature of adjustable load capacitors. It permits tuning of the circuit for initial tolerance of the crystal (often ± 20 ppm) as well as an adjustment for the required load capacitance (with possible variations from the PCB layout). While the oscillator was designed for a crystal with a nominal load capacitance of 12.5 pF, the circuit accommodates any value from ~ 7 pF to 22 pF (depending on parasitics of the layout). All of these corrections can be performed when the part is already installed on the PCB, in the actual circuit.

This adjustment can set the frequency of the crystal oscillator to within ± 4 ppm of the ideal value. As a reference, a typical 32.768 kHz crystal changes its frequency 4 ppm for a 10°C change in temperature. Since the temperature characteristics of crystals are well known and stable, the host processor is free to implement an algorithm for temperature compensation of the crystal oscillator using the adjustable load capacitors, with resulting accuracy of ± 4 ppm over the entire temperature range.

Using the ± 4 ppm, 32.768 kHz clock from the LF oscillator, the Real-Time Clock module keeps time with a maximum error as low as 2 minutes per year. This compares favorably with a conventional error of 2 minutes per month for the typical RTC chip.

All counting-chain values are loaded at the same time into corresponding registers when the Fractions register is read. All values from registers are loaded into the counting-chain when the Fractions register is written.

Figure 6. Real Time Clock and Periodic Interrupt / Wakeup timer

SYSTEM MANAGEMENT**Periodic Interrupt / Wakeup Timer**

Simple and versatile, the Periodic Interrupt / Wakeup Timer can be used to create very accurate recurring interrupts for use by the host micro. With some minimal software support from the host processor, it can also be used to create alarms, with practically unlimited duration.

While the timer is running, the host processor may be halted, consuming no energy. The interrupt wakes up the processor, which can perform the requisite task and go back to sleep, until the next periodic interrupt.

This mode of operation can achieve extremely low average power consumption.

A 32-bit counter clocked by 32.768 kHz, producing a minimum interval of 30.5 μ s and the maximum interval of 36.4 hours, creates the Timer.

After reset, the Timer is stopped until the new value for the time interval is written into the 4-byte Time Interval register. When the least significant byte (LSB) is written, the whole value is moved to the Time Interval latch, the counter is reset and starts to increment with the 32.768 kHz clock.

When the 32-bit comparator detects a match, an interrupt is generated and the counter is reset and starts the next timing cycle.

Although the counter cannot be written to, the current value from the counter can be read at any time. The whole 32-bit value is loaded into the 32-bit Current Timer Value latch when the least significant byte is read. This prevents errors stemming from the finite time between the readings of individual bytes of the current value.

Auxiliary functions**Scratchpad RAM**

Four (4) bytes of general-purpose RAM reside on the SH3003.

Voltage Regulator

Pin VREG can be used as a nominal 2.20 V reference voltage or a supply source for small loads (<2 mA). A bypass capacitor may be necessary between this pin and VSS if the load generates large current transients or a low ripple reference is required.

SYSTEM MANAGEMENT
Interrupt and Serial Interface

A single line is used to convey bi-directional information between the SH3003 and the processor, and as the interrupt line to the processor.

The polarity of the interrupt signal is programmable.

The SH3003 and the host microcontroller communicate using a single wire, bi-directional asynchronous serial interface. The bit rate is automatically determined by the SH3003. At the fastest possible rate, a read or write access of a single byte from the register bank takes 5 μ s.

The SH3003 contains 36 addressable registers located at 0x00–0x1F. Some of these registers are accessed through a page operation. Pin 14, IO/Int, is the serial communications interface and interrupt output pin. This pin is internally weakly pulled to the opposite of the programmed interrupt polarity. For example, if interrupt is programmed to be active low, this pin is weakly pulled to VDD when inactive.

As shown in **Figure 7**, the SH3003 and the host communicate with serial data streams. The host always initiates communication. A data stream consists of the following (in this order):

- 3-bit start field
- 3-bit read/write code
- 5-bit address field
- 1 guard bit
- 8-bit data field
- 2 parity bits

Plus, for write streams only:

- 1 guard bit
- 2 acknowledge (ACK) bits

The 3-bit start field (1,0,1 or 0,1,0, depending on interrupt polarity) uses the middle bit to determine the bit period of the serial data stream.

The 3-bit read/write code consists of 1,1,0 for a read, or 0,1,1 for a write. This protects against early glitches that might otherwise put the interface into an invalid read or write access mode.

The 5-bit address field contains the address of the register.

A single guard bit gives the interface a safe period in which to change data direction. The value of a guard bit does not matter.

The 8-bit data field is written to (read from) the register.

Two parity bits: The first parity bit is high when there are an odd number of bits in the read/write, address and data fields; the second parity bit is the inverse of the first.

For write streams only, a guard bit is appended to the stream (to allow safe turnaround), and then two acknowledge bits, which are a direct copy of the parity bits, are driven back to the host to indicate a successful write access.

Two guard bits are appended to the end of the access stream (read or write). The host can not start the next access before receiving these bits.

The interface is self-timed based on the duration of the start bit field, and communication can take place whenever CLKout is active, either at 32.768 kHz or at a higher frequency. If the host microcontroller is running synchronously to the CLKout generated by the SH3003 (which should generally be the case), then a minimum of 4 CLKout cycles per bit are required to maintain communication integrity. If the host's serial interface is asynchronous to CLKout, then a minimum of 52 cycles per bit are necessary. A maximum of 1024 CLKout cycles per bit field is supported.

Table 3 displays the minimum and maximum bit periods for the serial communications for CLKout frequencies of 16 MHz, 8 MHz, and 2 MHz.

Table 3: Minimum/Maximum Serial Bit Timing

CLKOUT Frequency	Minimum Bit Period (host synchronous to CLKOUT)	Minimum Bit Period (host asynchronous to CLKOUT)	Maximum Bit Period
16 MHz	250 ns	3.25 μ s	63.9 μ s
8 MHz	500 ns	6.5 μ s	127 μ s
2 MHz	2 μ s	26 μ s	511 μ s

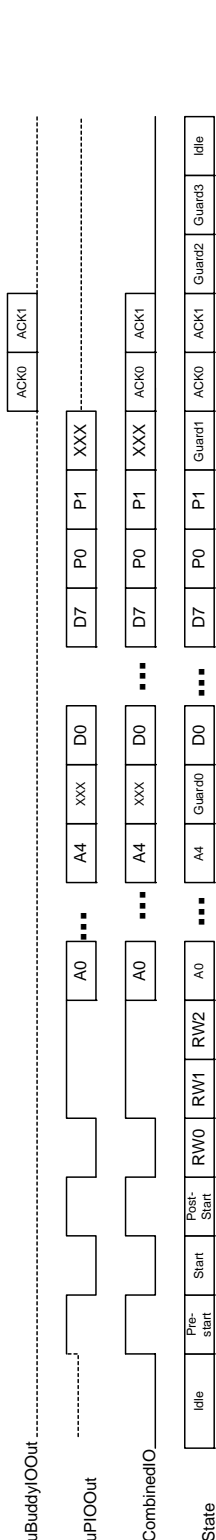
Interrupt Interface

The serial communications line to the SH3003 (Pin 14, IO/Int) also serves as the interrupt to the host microcontroller. The polarity of the interrupt is software programmable using the interrupt polarity bit (bit 6) of the IPol_RCTune register (R0x11). This pin is asserted for four cycles of CLKout, and then returns to the inactive state.

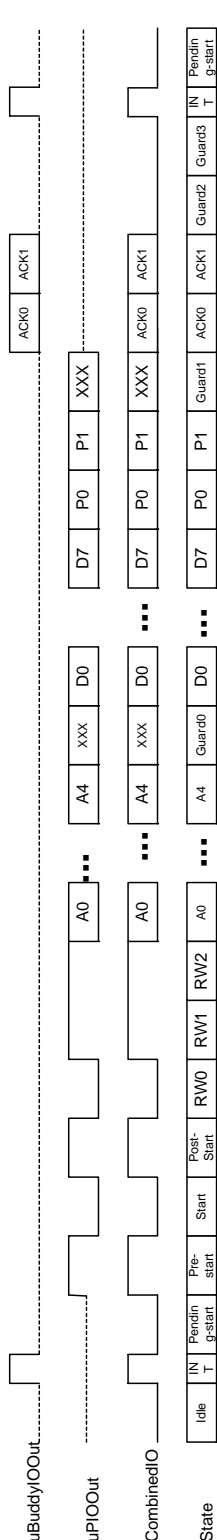
The interrupt line is used by the Periodic Interrupt/Wake-up Timer to interrupt the host when it reaches its end of count.

IO/INT timing scenarios

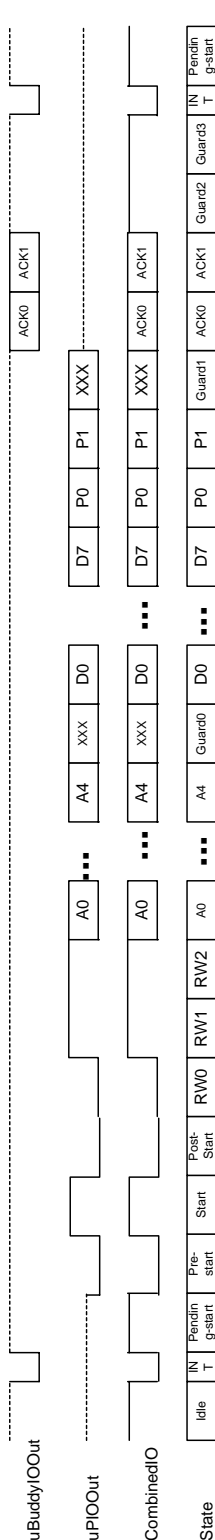
1. INT disabled, uP initiates write access. Active high interrupt.



2. INT active (high), uP initiates write access



3. INT active (low), uP initiates write access



4. INT disabled, uP initiates read access

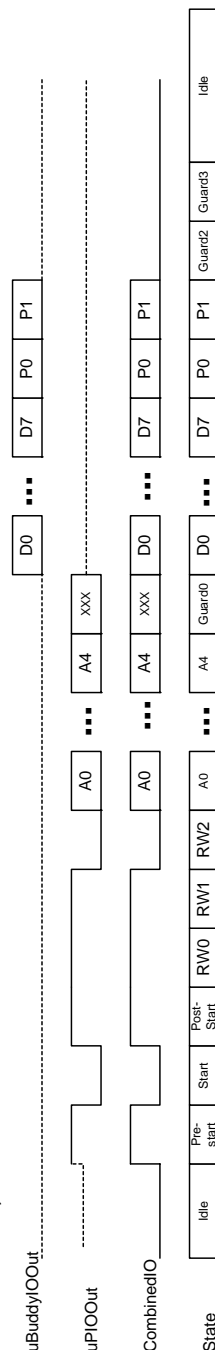


Figure 7: Serial Communication Timing Diagram

SYSTEM MANAGEMENT

Electrical Specifications

Absolute Maximum Ratings

Note: The SH3003 is ESD-sensitive.

Description	Symbol	Min	Max	Units
Supply voltages on VDD or VBAK relative to ground	VDD	-0.5	5.5	V
Input voltage on CLKIN, IO/INT, TEST	VIN1	-0.5	VDD + 0.5	V
Input voltage on CLKSEL	VIN2	-0.5	VREG + 0.5	V
Input current on any pin except VREG	IIN1		10	mA
Input current on VREG	IIN2		150	mA
Ambient operating temperature	TOP	-40	85	°C
Storage temperature	TSTG	-55	160	°C

Operating Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Notes
Case temperature	TOP	-40		+85	°C	
Supply voltage	VDD	2.3		5.5	V	
Supply current, CLKOUT = 16 MHz*	IDD			3	mA	
Supply current, CLKOUT = 8 MHz*	IDD		1.8		mA	
Supply current, CLKOUT = 2 MHz*	IDD		0.9		mA	
Standby current, 32.768 kHz crystal**	ISB			8	μA	CLK32 disabled
Standby current, 32.768 kHz RC oscillator**	ISB			10	μA	CLK32 disabled
Backup Supply Voltage**	VBAK	2.3		5.5	V	
Backup current, 32.768 kHz crystal**	IBUP			2	μA	CLK32 disabled
Backup current, 32.768 kHz RC oscillator **	IBUP			8	μA	CLK32 disabled
Backup standby current**	IBSB			50	nA	VDD > VBO

*Note: Assuming load on CLKOUT < 20 pf

**Note: Assuming temperature < 60°C

SYSTEM MANAGEMENT
Operating characteristics with crystal oscillator

Parameter	Symbol	Min	Typ	Max	Units
Crystal operating frequency	Fop		32.768		kHz
CLK32 duty cycle	DC	25		75	%
Startup time	Tst			3	secs
XIN/XOUT padding capacitance after power-up	Cpup		12.5		pF
Minimum XIN/XOUT padding capacitance	Cmin		10		pF
Maximum XIN/XOUT padding capacitance	Cmax		40		pF
Padding capacitance resolution	Cres		2		pF
XIN switching threshold	Vth		0.6		V
XIN to CLK32 delay	Td		0.5		μs
CLK32 frequency stability (crystal-dependent)	Fs		1		ppm/°C
CLK32 cycle to cycle jitter	J		0.05		%
CLK32 rise/fall time (10 pF load)	Trf		10		ns
CLK32 logic output low (0.5 mA load)	Vol		0.25	0.5	V
CLK32 logic output high (0.5 mA load)	Voh	-0.5	-0.25		Ref VDD*

*Note: VDD here is VDD during normal operation and VBAK during battery backup.

Operating characteristics of 32.768 kHz RC oscillator

Parameter	Symbol	Min	Typ	Max	Units
External 1 MOhm referenced nominal frequency	Fext		32.768		kHz
Internal 1 MOhm referenced nominal frequency	Fint		32.768		kHz
CLK32 duty cycle*	DC	40		60	%
Programmed frequency accuracy at 25°C	Fst	-1		+1	%
Absolute accuracy over temperature and supply (external 1 MOhm)	Fde		±2		%
Absolute accuracy over temperature and supply (internal 1 MOhm)	Fdi		±3		%
Frequency temperature stability (ext. 1 MOhm)	Fse		100		ppm/°C
Frequency temperature stability (int. 1 MOhm)	Fsi		200		ppm/°C
Power on startup time	Tst		70		μs
CLK32 cycle to cycle jitter*	J		0.1		%

*Note: After power-up, pin CLK32 is disabled, pin RREF is also disabled, and the oscillator is set to operate without the external reference resistor.

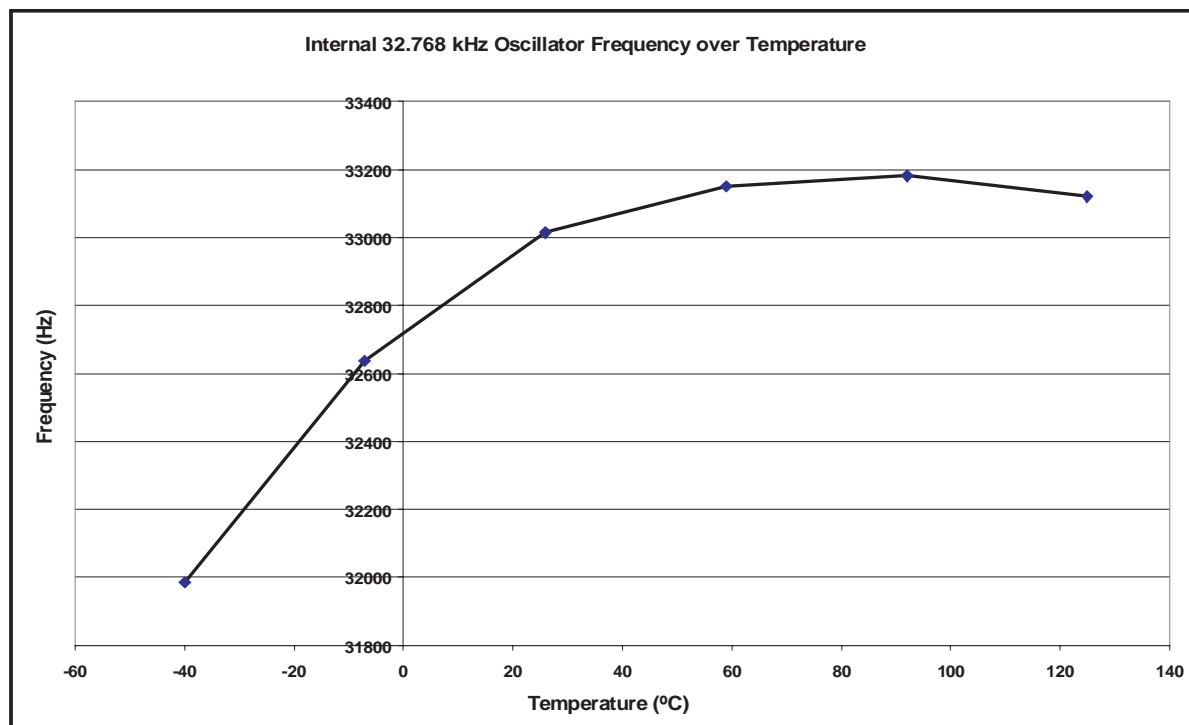
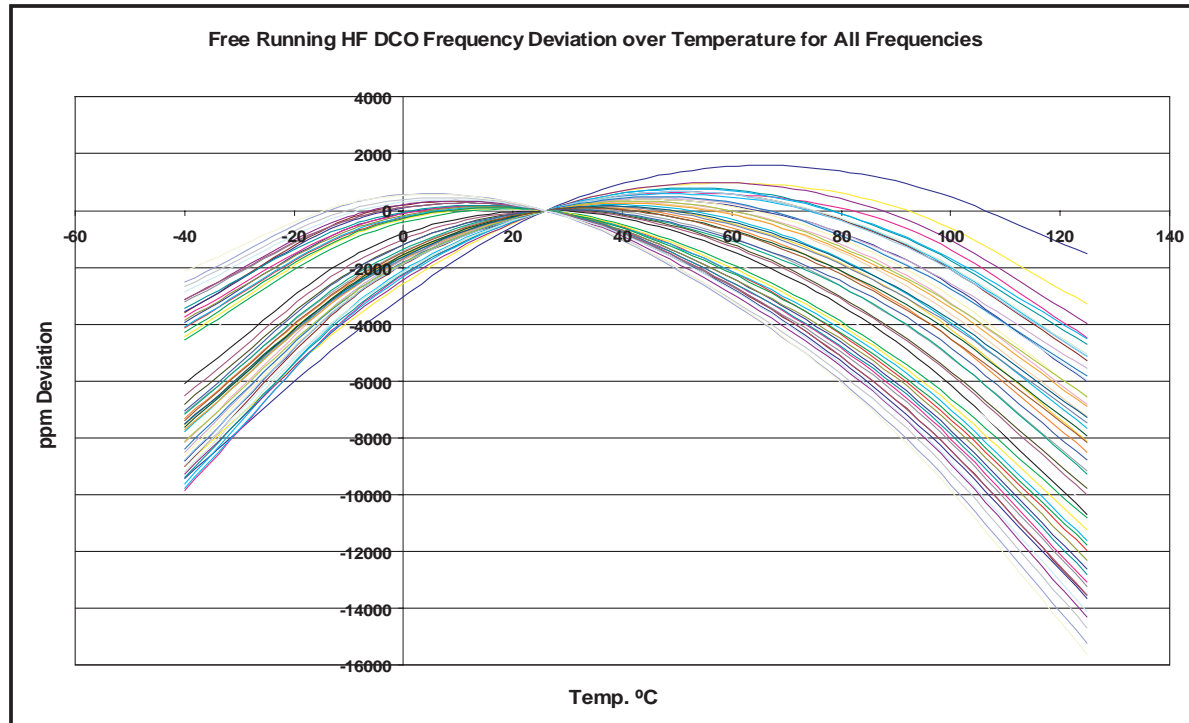
Operating characteristics of programmable reset

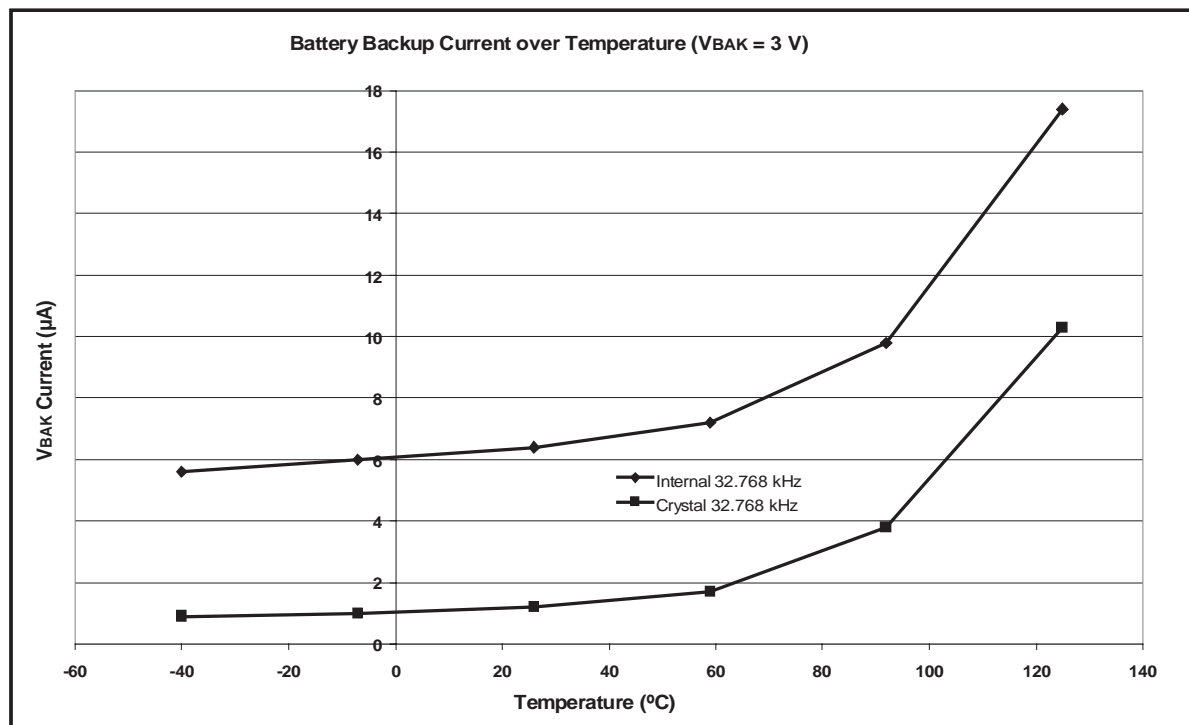
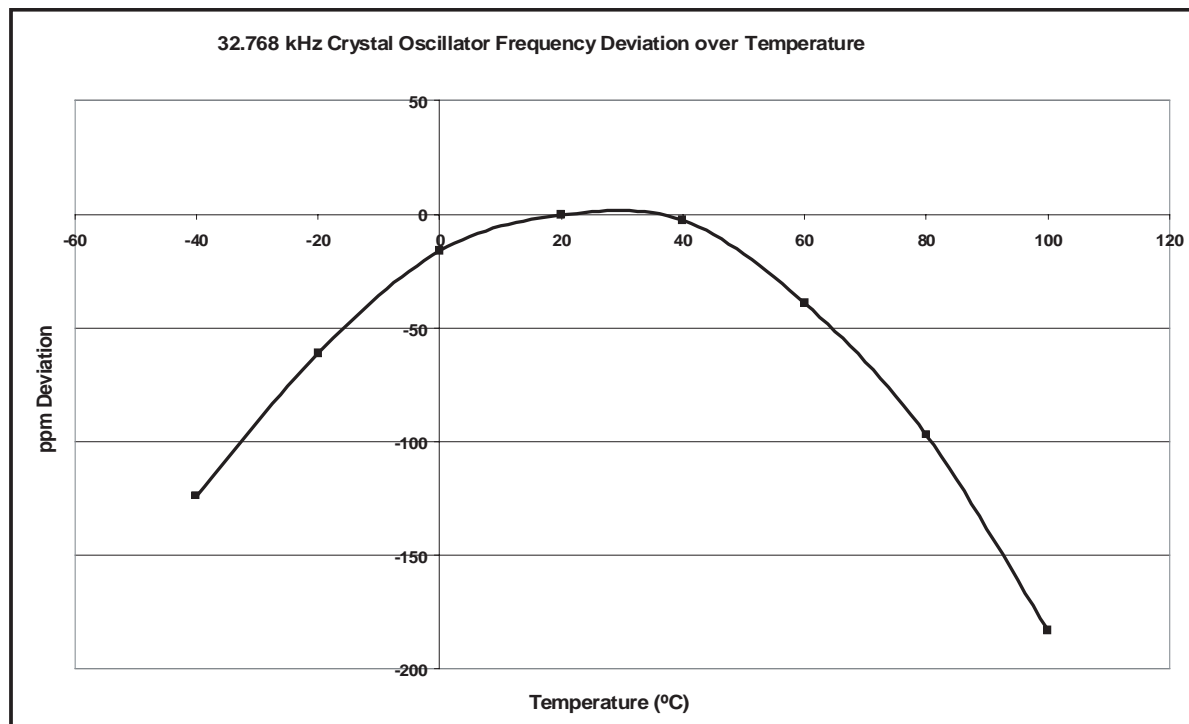
Parameter	Symbol	Min	Typ	Max	Units
VDD switching threshold after power-up	Vbo(pup)		2.3		V
VDD switching threshold for Min code	Vbo(min)	2.27	2.3	2.33	V
VDD switching threshold for Max code	Vbo(max)	4.2	4.3	4.4	V
VDD threshold resolution	Vres		33		mV
VDD hysteresis	Vhys		50		mV
Falling VDD threshold switch delay	Td		2.5		μs
Threshold digital-analog converter (DAC) settling time	Tdac		4		ms
Minimum VDD for valid NRST and RST	VDDmin			1	V

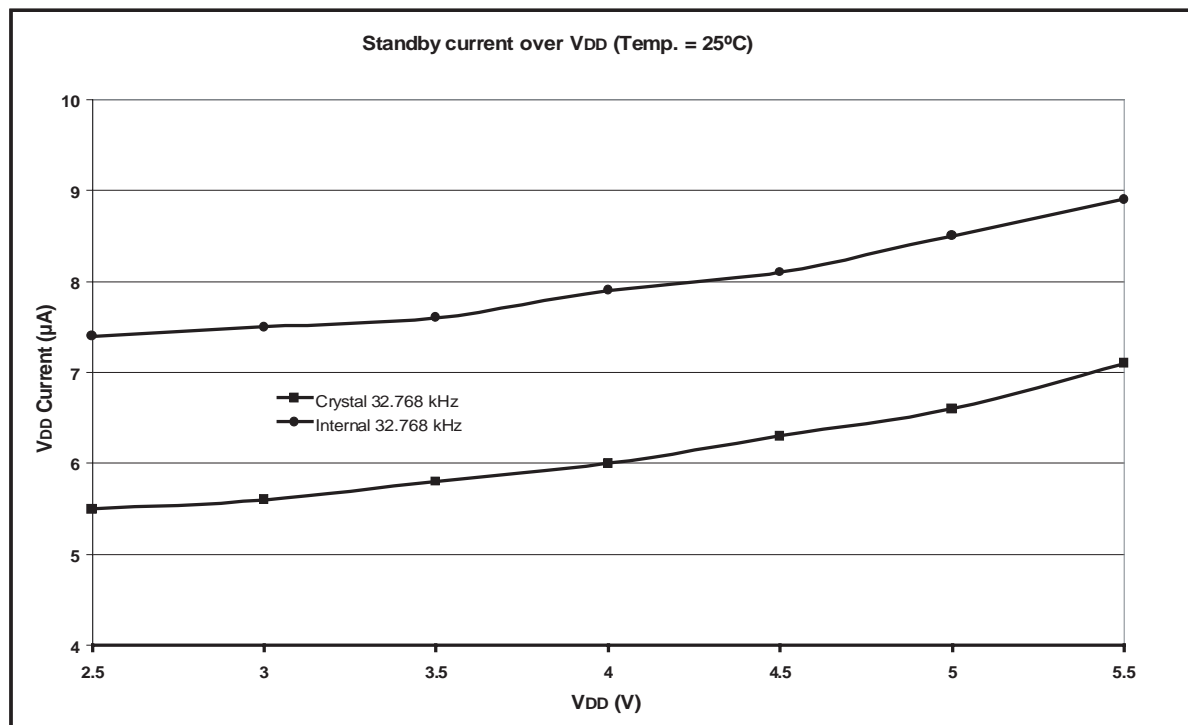
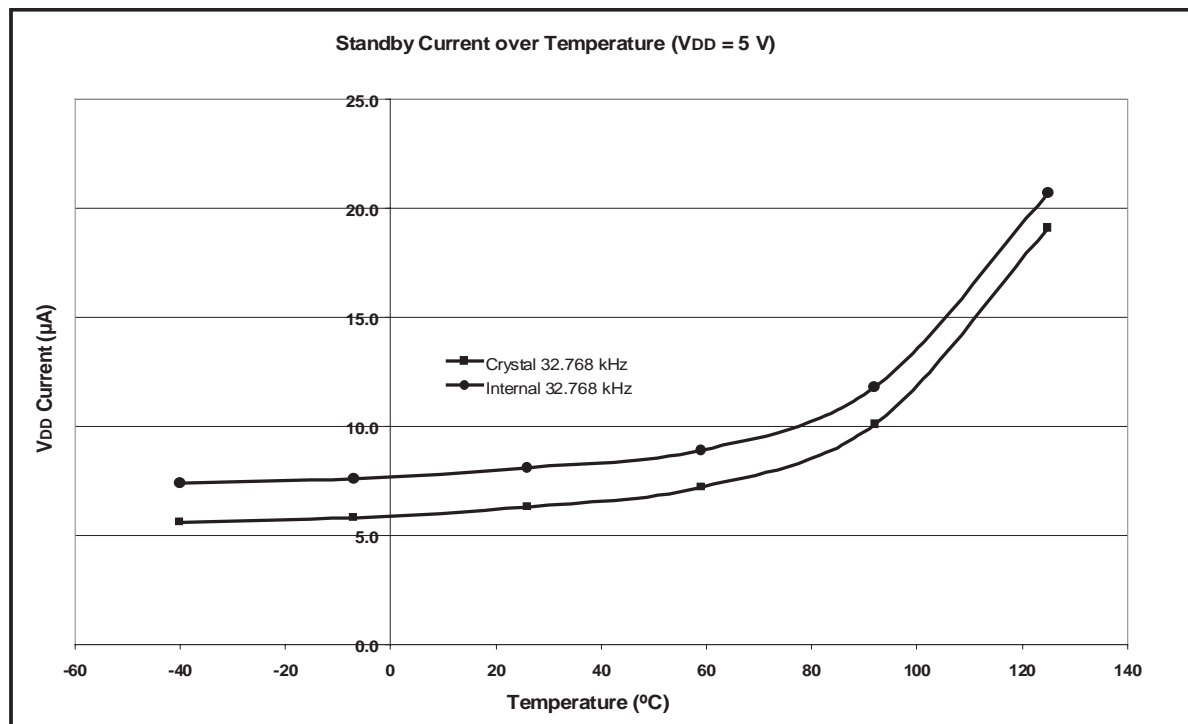
Operating characteristics of the high-frequency oscillator (HFO)

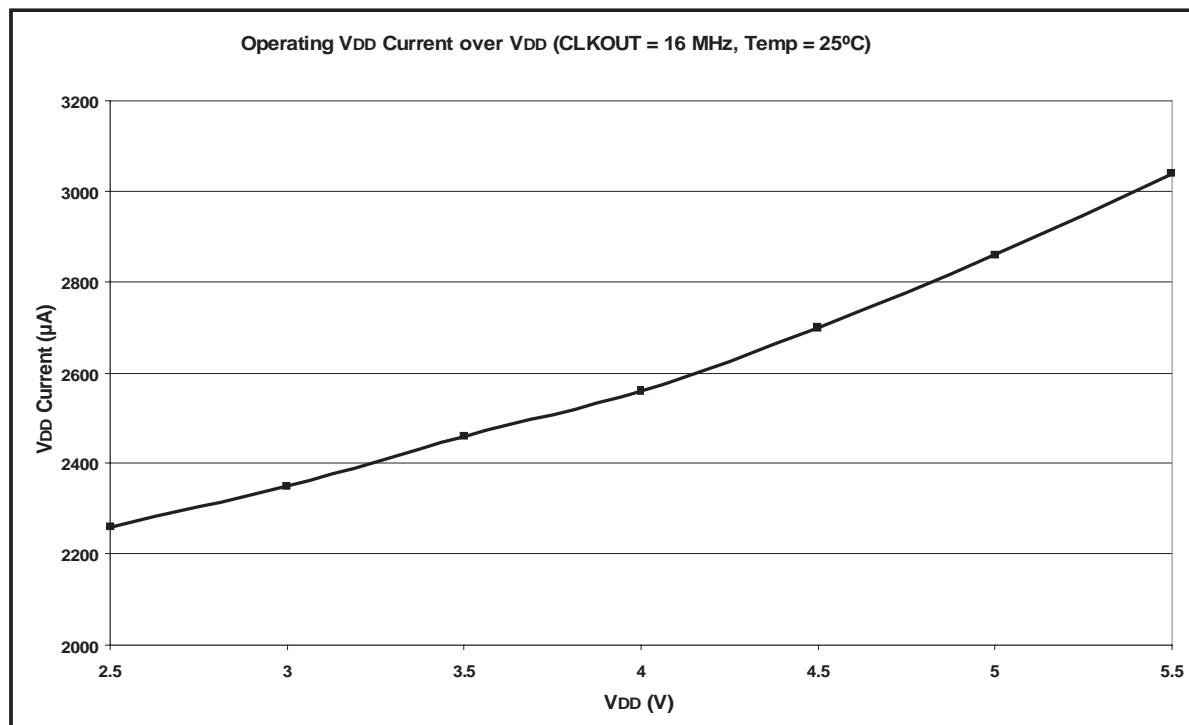
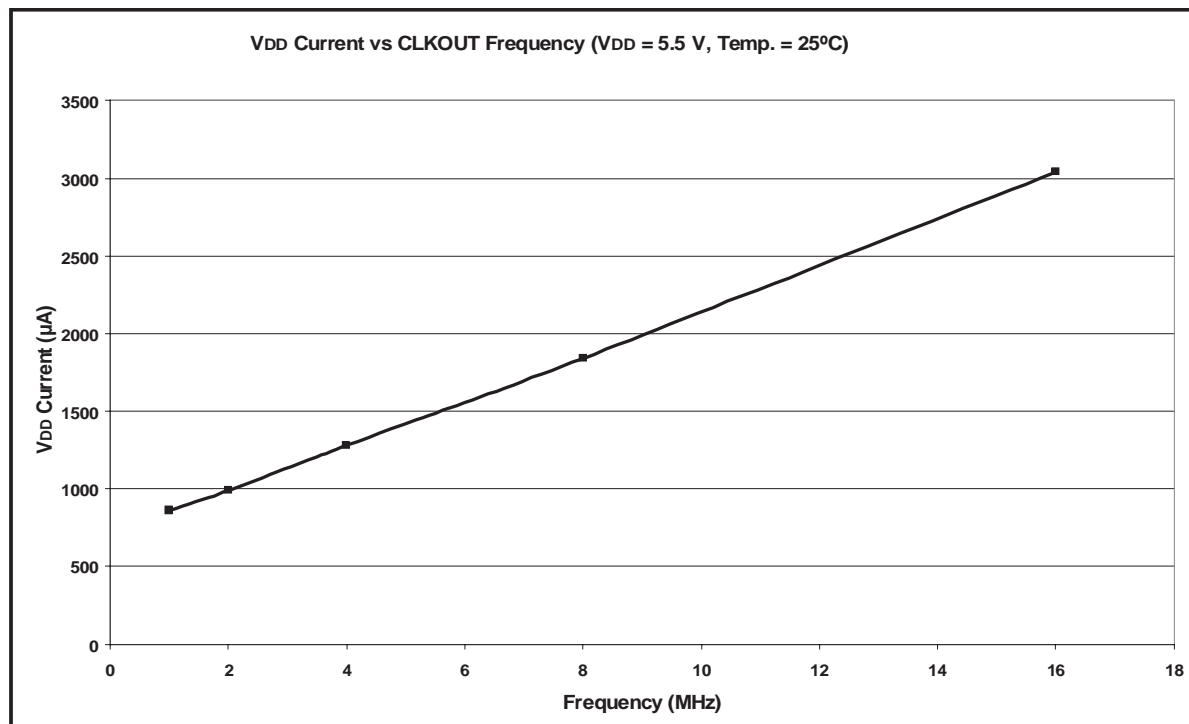
Parameter	Symbol	Min	Typ	Max	Units
Minimum operating frequency (start-up default = 16 MHz)	Fmin		5.6	8	MHz
Maximum operating frequency	Fmax	16.8	21		MHz
Frequency resolution	Fres		2		kHz
Programmed frequency accuracy at 25°C	Fst	-0.3		+0.3	%
Frequency drift over temperature and supply	Fdrift		±0.5		%
CLKOUT cycle to cycle jitter (spread spectrum off)	J		0.1		%
Startup time from standby	Tstart			2	μs
Settling time to 0.1% after HF digitally-controlled oscillator (DCO) code change	Tsett		10		μs
CLKOUT duty cycle	DC	40		60	%
Frequency temperature stability	Fts		100		ppm/°C
Short term frequency stability	Fs		0.5		%/sec
Minimum spread spectrum range*	SSmin		32		kHz
Maximum spread spectrum range*	SSmax		256		kHz
CLKOUT rise/fall time (20 pF load)	Trf		3		ns
CLKOUT logic output low (4 mA load)	Vol		0.25	0.4	V
CLKOUT logic output high (4 mA load)	Voh	-0.4	-0.25		Ref VDD

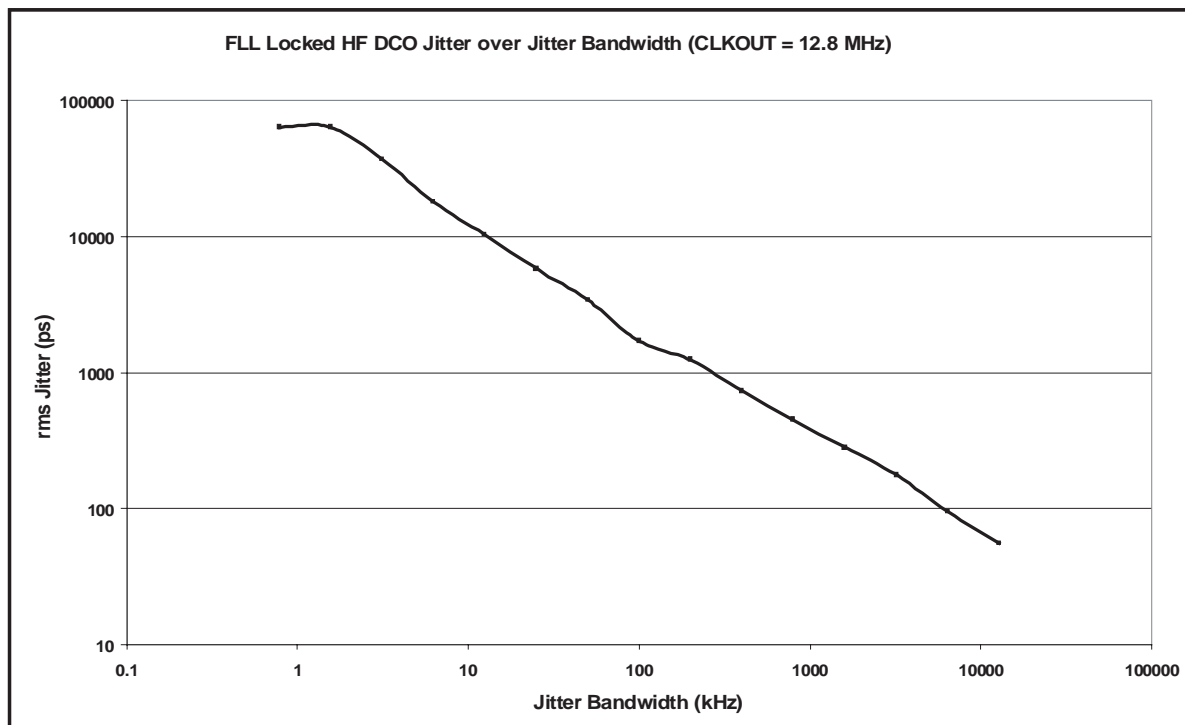
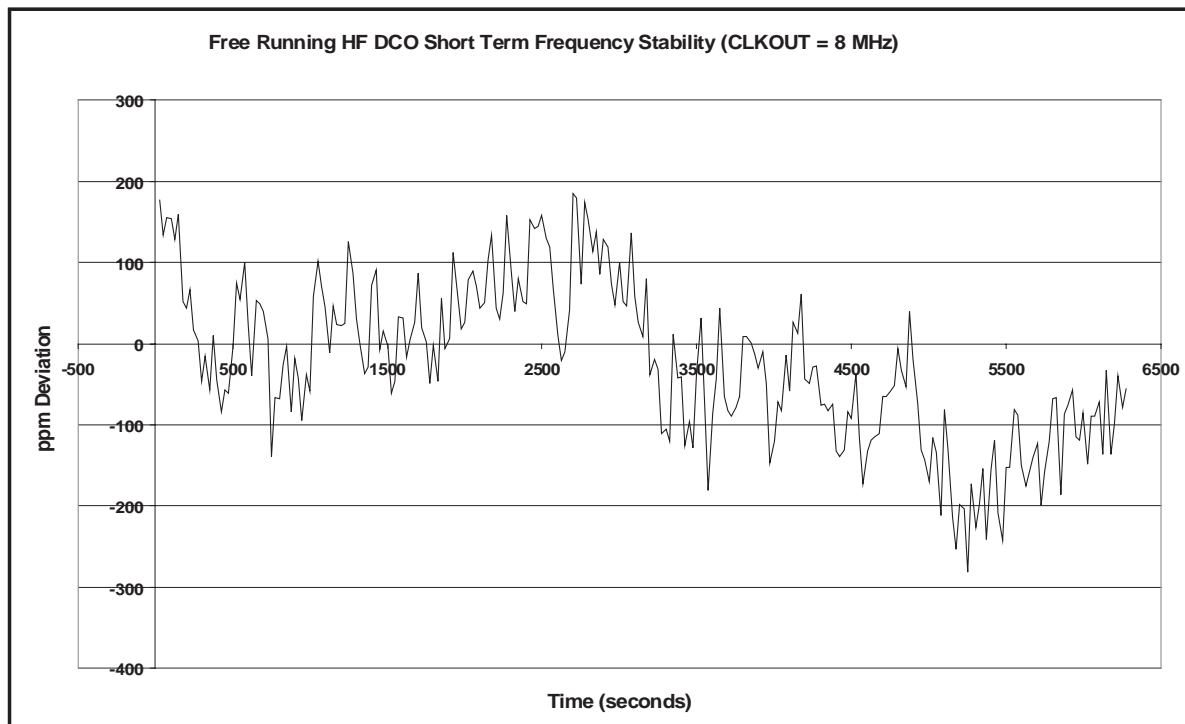
*Note: After power-up, spectrum spreading of the high-frequency oscillator is disabled.

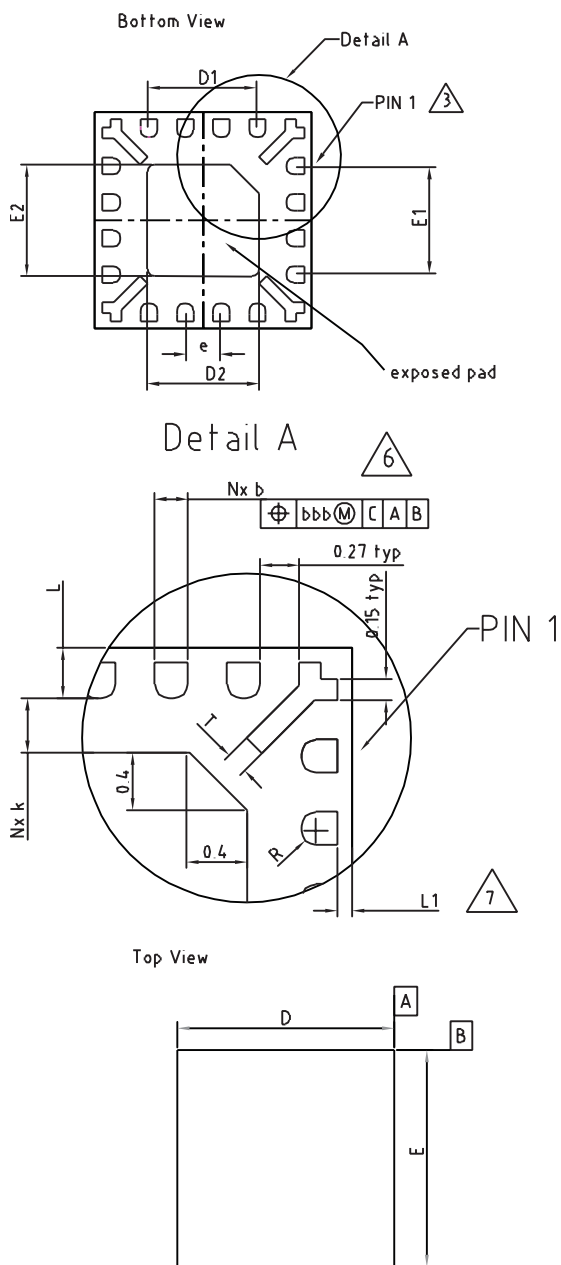
SYSTEM MANAGEMENT








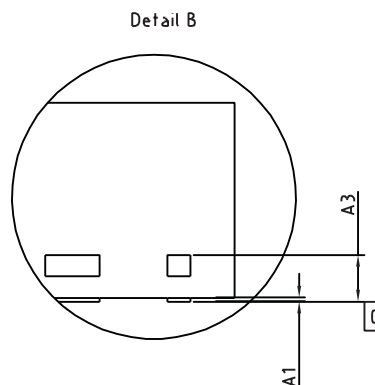


SYSTEM MANAGEMENT
Package Outline Drawing MLP 3 x 3 mm 16 pins

Notes

1. Reference JEDEC MO-220
2. All dimensions are in millimeters
3. Pin 1 orientation identified by chamfer on corner of exposed die pad
4. Datum C, the seating plane, is defined by the flat surface of the metallized terminal
5. Dimension 'e' represents the terminal pitch
6. Dimension 'b' applies to the metallized terminal and is measured 0.25 to 0.3 mm from terminal tip
7. Dimension L1 represents terminal pull back from package edge. Where terminal pull back exists, only upper half of lead is visible on package edge due to half etching of leadframe
8. Leadframe material is copper A194
9. Coplanarity applies to the exposed pad as well as the terminals
10. Tolerance for Form & Position, bbb = 0.10 mm

Common Dimensions (mm)

Sym	Min	Nom	Max
A	0.8	0.9	1.0
A1	0	0.02	0.05
A3		0.2 REF	
D	2.9	3.0	3.1
D1		1.5	
D2	1.45	1.55	1.65
E	2.9	3.0	3.1
E1		1.5	
E2	1.45	1.55	1.65
L	0.3	0.35	0.4
L1			0.1
b	0.18	0.23	0.3
N		16	
e		0.5	
K	0.2		
R	bmin/2		
T		0.25	



**For sales information and product literature,
contact:**

Semtech Corporation
Human Interface Device (HID)
and System Management Division
200 Flynn Road
Camarillo, CA 93012-8790
<http://www.semtech.com/>
(805)498-2111 Telephone
(805)498-3804 Fax

Copyright ©2002-2005 Semtech Corporation. All rights reserved. Semtech, the Semtech logo, MicroBuddy, µBuddy, and µB are marks of Semtech Corporation. All other marks belong to their respective owners.

Changes may be made to this product without notice. Customers are advised to obtain the latest version of the relevant information before placing orders.

LIMITED LICENSE GRANTED: NO WARRANTIES MADE

This specification is provided "as is" with no warranties whatsoever including any warranty of merchantability, fitness for any particular purpose, or any warranty otherwise arising out of any proposal, specification or sample. Any suggestions or comments by Semtech concerning use of this product are opinion only, and Semtech makes no warranty as to results to be obtained in any specific application. A license is hereby granted to reproduce and distribute this specification for internal use only. No other license, expressed or implied to any other intellectual property rights is granted or intended hereby. Authors of this specification disclaim any liability, including liability for infringement of proprietary rights, relating to the implementation of information in this specification. Authors of this specification also do not warrant or represent that such implementation(s) will not infringe such rights.