SC1205
High Speed Synchronous Power MOSFET Driver

Description

The SC1205 is a cost effective Dual MOSFET Driver designed for switching High and Low side Power MOSFETs. Each driver is capable of driving a 3000pF load in 20ns max rise/fall time and has a 20ns max propagation delay from input transition to the gate of the power FET's. An internal Overlap Protection circuit prevents shoot-through from Vin to GND in the main and synchronous MOSFET's. The Adaptive Overlap Protection circuit ensures the Bottom FET does not turn on until the Top FET source has reached a voltage low enough to prevent cross-conduction.

The high current drive capability (3A peak) allows fast switching, thus reducing switching losses at high (up to 1MHz) frequencies without overheating the driver. The high voltage CMOS process allows operation from 5-25 Volts at top MOSFET drain, thus making SC1205 suitable for battery powered applications. Connecting Enable pin (EN) to logic low shuts down both drives and reduces operating current to less than 10uA.

An Under-Voltage-Lock-Out circuit is included to guarantee that both driver outputs are low when the 5V logic level is less than or equal to 4.4V (typ) at supply ramp up (4.35V at supply ramp down). An Internal temperature sensor shuts down all drives in the event of overtemperature. SC1205 is fabricated utilizing Bi-CMOS technology for low quiescent current. The SC1205 is offered in a standard SO-8 package.

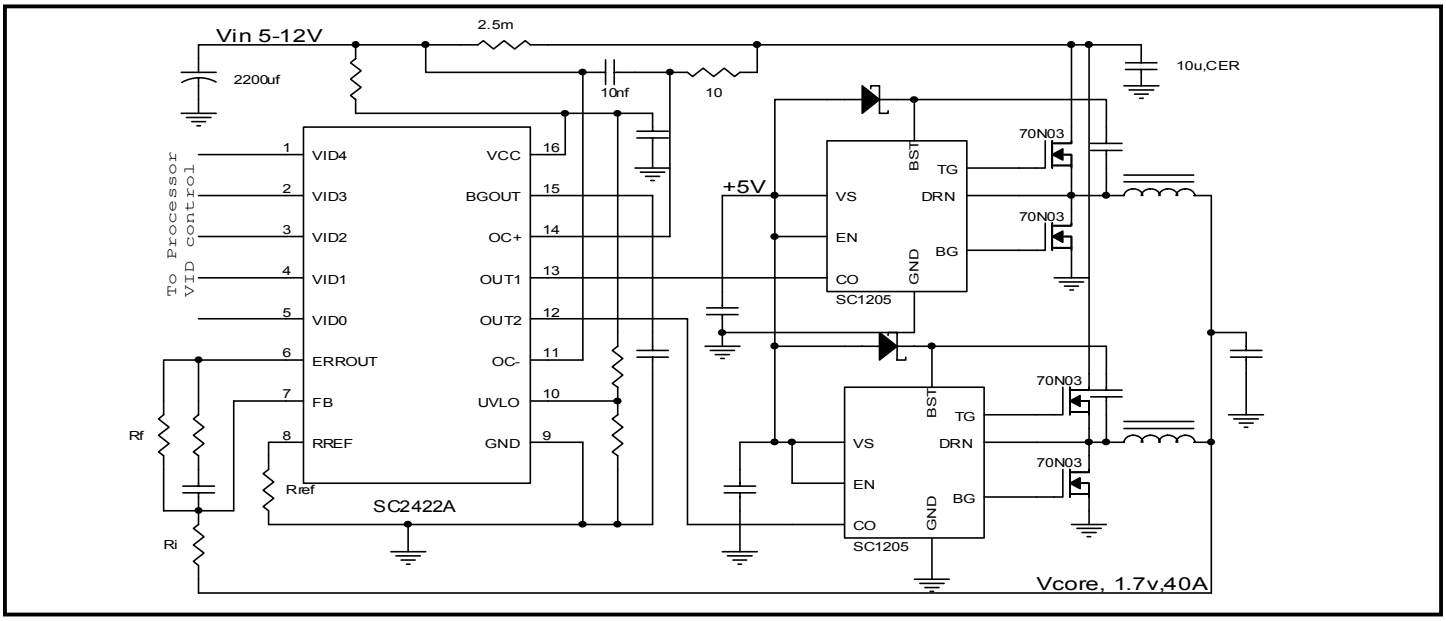
Features

- Fast rise and fall times (15ns typical with 3000pf load)
- **3 Amp peak drive current**
- 14ns max Propagation delay (BG going low)
- Adaptive Non-overlapping Gate Drives provide shoot-through protection
- Floating top drive switches up to 25V
- Under-Voltage lock-out
- Overtemperature protection
- Less than 10µA supply current when EN is low
- Low cost

Applications

- High Density sunchronous power supplies
- Motor Drives/Class-D amps/Half bridge drivers
- High frequency (to 1.2 MHz) operation allows use of small inductors and low cost caps in place of electrolytics
- High efficiency portable computers
- Battery powered applications

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Conditions	Maximum	Units
V_{CC} Supply Voltage	V_{IMAXSW}		7	V
BST to PGND	$VMAX_{BST-PGND}$		30	V
BST to DRN	$VMAX_{BST-DRN}$		7	V
DRN to PGND	$VMAX_{DRN-PGN}$		-2 to 25	V
DRN to PGND Pulse	$VMAX_{PULSE}$	t_{PULSE} < 100ns	-5 to 25	V
OVP_S to PGND	$VMAX_{OVP\ S-PGND}$		10	V
Input Pin	CO		-0.3 to 7.3	V
Continuous Power Dissipation	Pd	Tamb = 25°C, T_J = 125°C Tcase = 25°C, T_J =125°C	0.66 2.56	W
Thermal Resistance Junction to Case	θ_{JC}		40	°C/W
Thermal Resistance Junction to Ambient	θ_{JA}		150	°C/W
Operating Temperature Range	T_J		0 to +125	°C
Storage Temperature Range	T_{STG}		-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}		300	°C

NOTE:
(1) Specification refers to application circuit in Figure 1.

Electrical Characteristics

Unless specified: -0 < θ_J < 125°C; V_{CC} = 5V; 4V < V_{BST} < 26V

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Supply						
Supply Voltage	V_{CC}	V_{CC}	4.15	5	6.0	V
Quiescent Current, Operating	Iq_op	V_{CC} = 5V, C_O = OV		1		mA
Quiescent Current	Iq_stby	EN = OV			10	µA
Under Voltage Lockout						
Start Threshold	V_{START}		4.2	4.4	4.6	V
Hysteresis	$Vhys_{UVLO}$			0.05		V
Logic Active Threshold	V_{ACT}				1.5	V
EN						
High Level Input Voltage	V_{IH}		2.0			V
Low Level Input Voltage	V_{IL}				0.8	V

Electrical Characteristics (Cont.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
CO						
High Level Input Voltage	V_{IH}		2.0			V
Low Level Input Voltage	V_{IL}				0.8	V
Thermal Shutdown						
Over Temperature Trip Point	T_{OTP}			165		°C
Hysteresis	T_{HYST}			10		°C
High Side Driver						
Peak Output Current	I_{PKH}			3		A
Output Resistance	$Rsrc_{TG}$ $Rsink_{TG}$	duty cycle < 2%, tpw < 100 µs, T_J = 125°C, V_{BST} - V_{DRN} = 4.5V, V_{TG} = 4.0V (src) +V_{DRN} or V_{TG} = 0.05V (sink) +V_{DRN}		1 .7		Ω
Low-Side Driver						
Peak Output Current	I_{PKL}			3		A
Output Resistance	$Rsrc_{BG}$ $Rsink_{BG}$	duty cycle < 2%, tpw < 100 µs, T_J = 125°C, V_{VS} = 4.6V, V_{BG} = 4V (src), or V_{LOWDR} = 0.5V (sink)		1.2 1.0		Ω Ω

AC Operating Specifications

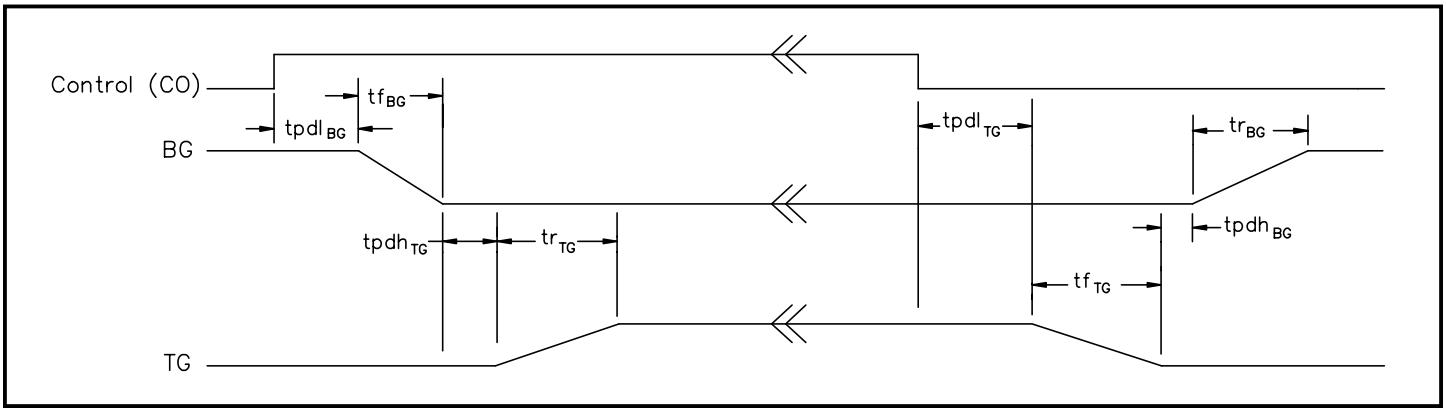
Parameter	Symbol	Conditions	Min	Typ	Max	Units
High Side Driver						
Rise Time	tr_{TG1}	Cl = 3nF, V_{BST} - V_{DRN} = 4.6V, **T_J + 125°C**		14	**23**	ns
Fall Time	tf_{TG}	Cl = 3nF, V_{BST} - V_{DRN} = 4.6V, **T_J + 125°C**		12	**19**	ns
Propagation Delay Time, TG Going High	$tpdh_{TG}$	Cl = 3nF, V_{BST} - V_{DRN} = 4.6V, **T_J + 125°C**		20	**32**	ns
Propagation Delay Time, TG Going Low	$tpdl_{TG}$	Cl = 3nF, V_{BST} - V_{DRN} = 4.6V, **T_J + 125°C**		15	**24**	ns
Low-Side Driver						
Rise Time	tr_{BG}	Cl = 3nF, V_{VS} = 4.6V, **T_J + 125°C**		15	**24**	ns

Note:
(1) This device is ESD sensitive. Use of standard ESD handling precautions is required.

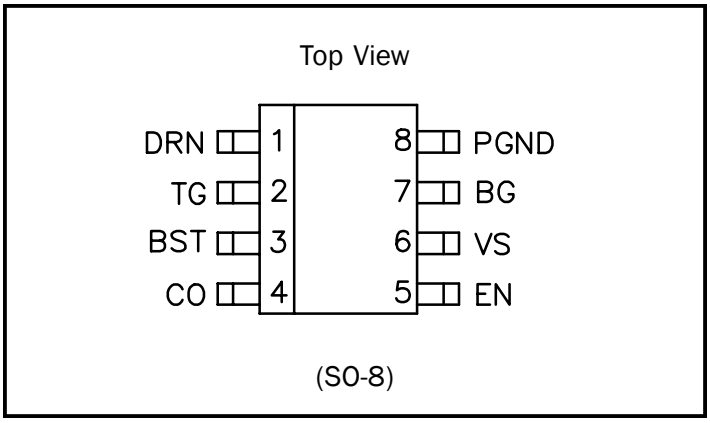
AC Operating Specifications (Cont.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Low-Side Driver						
Fall Time	tr_{BG}	Cl = 3nF, V_{VS} = 4.6V, **T_J + 125°C**		13	**21**	ns
Propagation Delay Time BG Going High	$tpdh_{BGHI}$	Cl = 3nF, V_{VS} = 4.6V, **T_J + 125°C**		12	**19**	ns
Propagation Delay Time BG Going Low	$tpdl_{BGHI}$	Cl = 3nF, V_{VS} = 4.6V, **T_J + 125°C**		7	**12**	ns
Under-Voltage Lockout						
V_5 ramping up	$tpdh_{UVLO}$	EN is High			10	µs
V_5 ramping down	$tpdL_{UVLO}$	EN is High			10	µs

Timing Diagrams



Pin Configuration



Ordering Information

Device [1]	Package	Temp Range (T_J)
SC1205CS.TR	SO-8	0° to 125°C
SC1205CSTRT[2]		

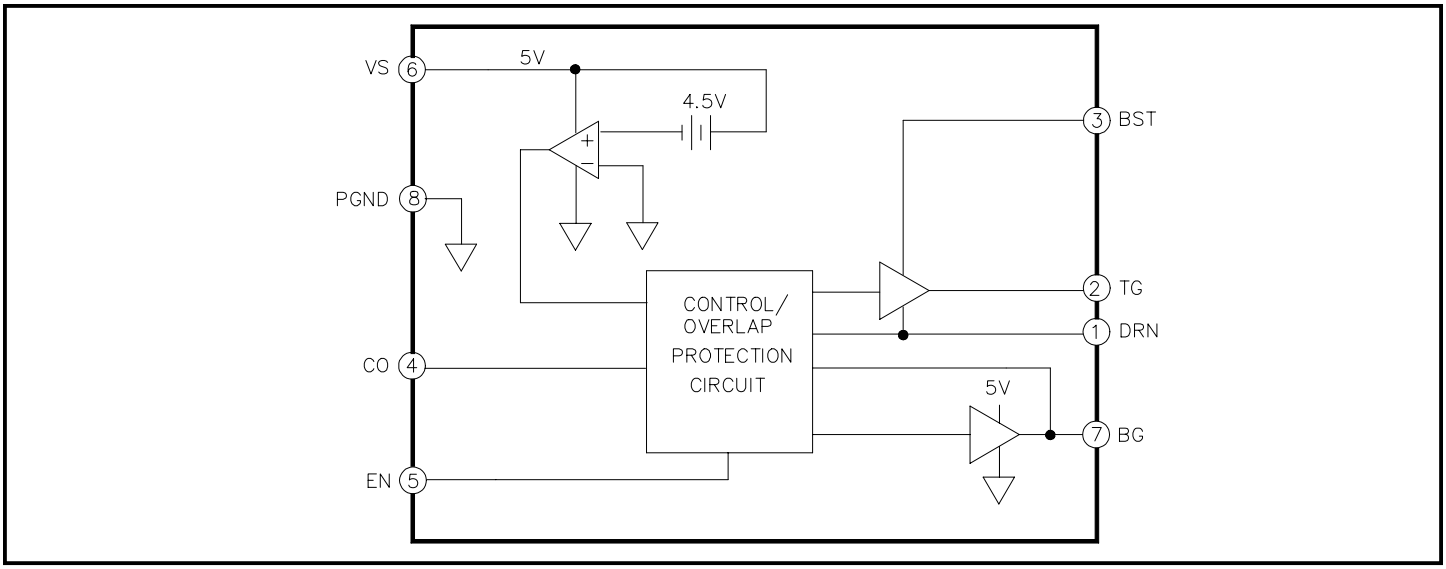
Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Lead free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	DRN	This pin connects to the junction of the switching and synchronous MOSFET's. This pin can be subjected to a -2V minimum relative to PGND without affecting operation.
2	TG	Output gate drive for the switching (high-side) MOSFET.
3	BST	Bootstrap pin. A capacitor is connected between BST and DRN pins to develop the floating bootstrap voltage for the high-side MOSFET. The capacitor value is typically between 0.1µF and 1µF (ceramic).
4	CO	TTL-level input signal to the MOSFET drivers.
5	EN	When high, this pin enables the internal circuitry of the device. When low, TG and BG are forced low and the supply current (5V) is less than 10µA.
6	VS	+5V supply. A .22-1µF ceramic capacitor should be connected from 5V to PGND very close to this pin.
7	BG	Output drive for the synchronous (bottom) MOSFET.
8	PGND	Ground.

NOTE:
(1) All logic level inputs and outputs are open collector TTL compatible.

Block Diagram



Applications Information

SC1205 is a high speed, smart dual MOSFET driver. It is designed to drive Low Rds_On power MOSFET's with ultra-low rise/fall times and propagation delays. As the switching frequencies of PWM controllers is increased to reduce power supply volume and cost, fast rise and fall times are necessary to minimize switching losses (TOP MOSFET) and reduce Dead-time (BOTTOM MOSFET). While Low Rds_On MOSFET's present a power saving in I^2R losses, the MOSFET's die area is larger and thus the effective input gate capacitance of the MOSFET is increased. Often a 50% decrease in Rds_On more than doubles the effective input gate charge, which must be supplied by the driver. The Rds_On power savings can be offset by the switching and dead-time losses with a sub_optimum driver. While discrete solutions can achieve reasonable drive capability, implementing shoot-through and other housekeeping functions necessary for safe operation can become cumbersome and costly. The SC120X family of parts presents a total solution for the high-speed high power density applications. Wide input supply range of 4.5V-25V allows use in battery powered applications, new high voltage, distributed power servers as well as Class-D amplifiers.

THEORY OF OPERATION

The control input (CO) to the SC1205 is typically supplied by a PWM controller that regulates the power supply output. (See Application Evaluation Schematic, Figure 4). The timing diagram demonstrates the sequence of events by which the top and bottom drive signals are applied. The shoot-through protection is implemented by holding the bottom FET off until the voltage at the phase node (intersection of top FET source, the output inductor and the bottom FET drain) has dropped below 1V. This assures that the top FET has turned off and that a direct current path does not exist between the input supply and ground. The top FET Gate Drive is turned on after the bottom gate drive has gone low and an internal delay time of 20ns has expired.

LAYOUT GUIDELINES

As with any high speed , high current circuit, proper layout is critical in achieving optimum performance of the SC1205. The Evaluation board schematic (Refer to figure 3) shows a two-phase synchronous design with all surface mountable components.

While components connecting to EN are relatively non-critical, tight placement and short, wide traces must be used in layout of The gate drives, DRN, and especially PGND pin. The top gate driver supply voltage is provided by bootstrapping the +5V supply and adding it to the phase node (DRN) voltage . Since the bootstrap capacitor supplies the charge to the top gate, it must be less than .5" away from the SC1205. Ceramic X7R capacitors are a good choice for supply bypassing near the chip. The Vcc pin capacitor must also be less than .5" away from the SC1205. The ground node of this capacitor,

the SC1205 PGND pin and the Source of the bottom FET must be very close to each other, preferably with common PCB copper land with multiple vias to the ground plane (if used). The parallel Schottky (if used) must be physically next to the Bottom FET's drain and source pins. Any trace or lead inductance in these connections will drive current way from the Schottky and allow it to flow through the FET's Body diode, thus reducing efficiency.

Preventing Inadvertent Bottom FET Turn-on

At high input voltages, (12V and greater) a fast turn-on of the top FET creates a positive going spike on the Bottom FET's gate through the Miller capacitance, Crss of the bottom FET. The voltage appearing on the gate due to this spike is:

$$V_{SPIKE} = \frac{Vin * crss}{(Crss + ciss}$$

Where Ciss is the input gate capacitance of the bottom FET. This is assuming that the impedance of the drive path is too high compared to the instantaneous impedance of the capacitors. (since dV/dT and thus the effective frequency is very high). If the BG pin of the SC1205 is very close to the bottom FET, Vspike will be reduced depending on trace inductance, rate of rise of current, etc.

While not shown in Figure 4, a capacitor may be added from the gate of the Bottom FET to its source, preferably less than .5" away. This capacitor will be added to Ciss in the above equation to reduce the effective spike voltage.

The bottom MOSFET must be selected with attention paid to the Crss/Ciss ratio. A low ratio reduces the Miller feedback and thus reduces Vspike. Also MOSFETs with higher Turn-on threshold voltages will conduct at a higher voltage and will not turn on during the spike. The MOSFET shown in the schematic (Figure 4) has a 2 volt threshold and will require approximately 4.5 volts Vgs to be conducting, thus reducing the possibility of shoot-through. A zero ohm bottom FET gate resistor will obviously help keeping the gate voltage low during off time.

Ultimately, slowing down the top FET by adding gate resistance will reduce di/dt which will in turn make the effective impedance of the capacitors higher, thus allowing the BG driver to hold the bottom gate voltage low. It does this at the expense of increased switching times (and switching losses) for the top FET.

RINGING ON THE PHASE NODE

The top MOSFET source must be close to the bottom MOSFET drain to prevent ringing and the possibility of the phase node going negative. This frequency is determined by:

$$Fring = \frac{1}{(2\Pi * Sqrt\ (L_{ST} * Coss)}$$

Where:

L_{st} = The effective stray inductance of the top FET added to trace inductance of the connection between top FET's source and the bottom FET's drain added to the trace resistance of the bottom FET's ground connection.
Coss=Drain to source capacitance of bottom FET. If there is a Schottky used, the capacitance of the Schottky is added to this value.

Although this ringing does not pose any power losses due to a fairly high Q, it could cause the phase node to go too far negative, thus causing improper operation, double pulsing or at worst driver damage. On the SC1205, the drain node, DRN, can go as far as 2V below ground without affecting operation or sustaining damage.

The ringing is also an EMI nuisance due to its high resonant frequency. Adding a capacitor, typically 1000-2000pf, in parallel with Coss of the bottom FET can often eliminate the EMI issue. If double pulsing, due to excessive ringing, placing a 4.7-10 ohm resistor between the phase node and the DRN pin of the SC1205 should eliminate the double pulsing.

The negative voltage spikes on the phase node adds to the bootstrap capacitor voltage, thus increasing the voltage between VBST - VDRN. If the phase node negative spikes are too large, the voltage on the boost capacitor could exceed device's absolute maximum rating of 7V. To eliminate the effect of the ringing on the boost capacitor voltage, place a 4.7 - 10 Ohm resistor between boost Schottky diode and Vcc to filter the negative spikes on DRN Pin. Alternately, a Silicon diode, such as the commonly available 1N4148 can substitute for the Schottky diode and eliminate the need for the series resistor.

Applications Information (Cont.)

Proper layout will guarantee minimum ringing and eliminate the need for external components. Use of SO-8 or other surface mount MOSFETs while increasing thermal resistance, will reduce lead inductance as well as radiated EMI.

Over Temp Shutdown

The SC1205 will shutdown by pulling both driver if its junction temperature, T_J, exceeds 165 °C.

Typical Performance Plots

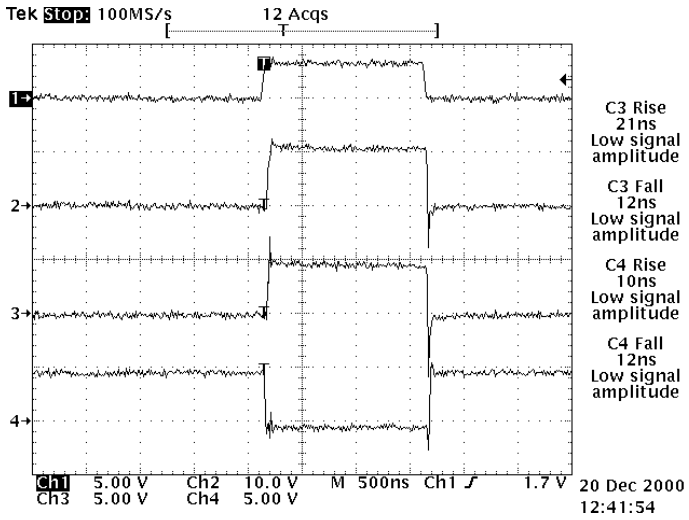


Figure 1: PWM input and Gate drive switching waveforms. The MOSFETs driven are FDB7030BL . See Figure 4 (Evaluation Board Schematic)
Ch1: PWM input signal
Ch2: Top Gate Drive
Ch3: Phase (Switching) Node
Ch4: Bottom Gate

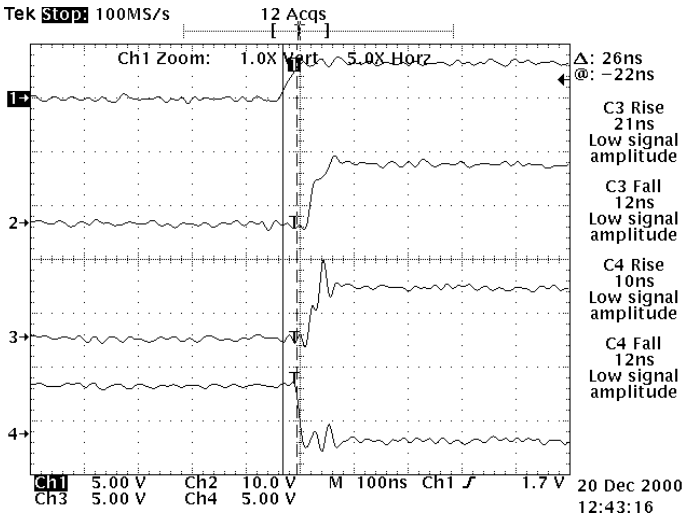


Figure 2: PWM input and Gate drive and phase node switching waveforms with time scale expanded. The MOSFETs driven are FDB7030BL . See Figure 4 (Evaluation Board Schematic)
Ch1: PWM input signal
Ch2: Top Gate Drive
Ch3: Phase (Switching) Node
Ch4: Bottom Gate

Typical Performance Plots

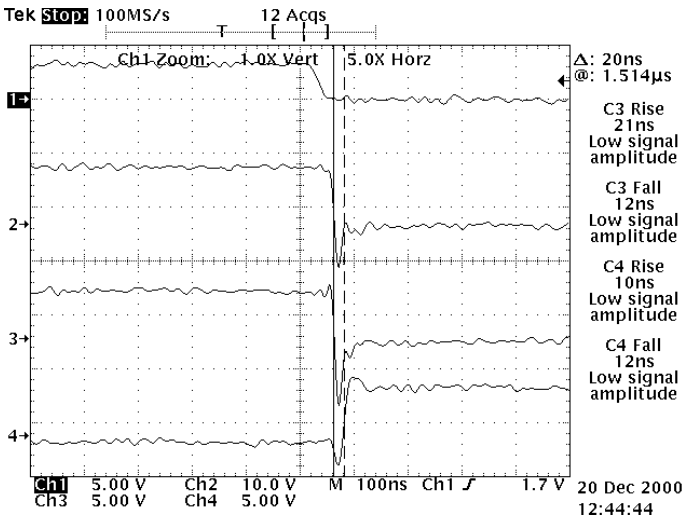
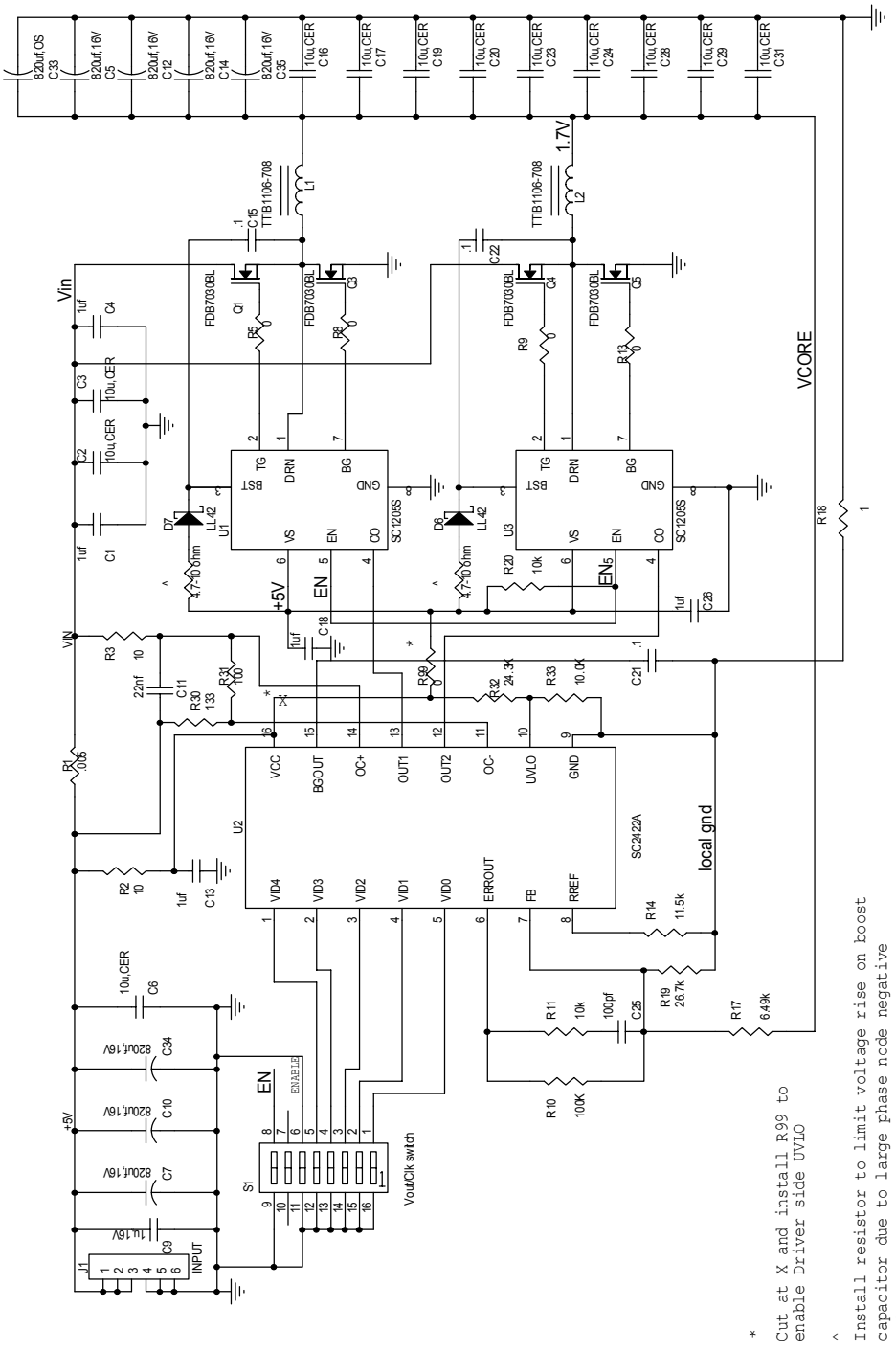


Figure 3: PWM input and Gate drive and phase node switching waveforms with time scale expanded. The MOSFETs driven are FDB7030BL . See Figure 4 (Evaluation Board Schematic)
Ch1: PWM input signal
Ch2: Top Gate Drive
Ch3: Phase (Switching) Node
Ch4: Bottom Gate

Evaluation Board Schematic - 3SC1205

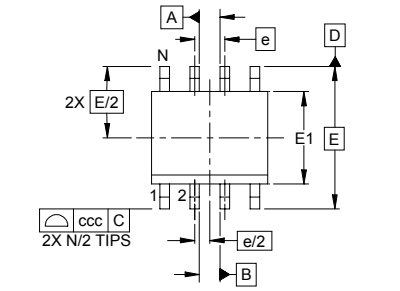
Figure 4- Microprocessor Core Supply

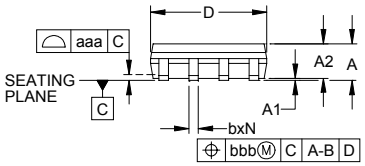


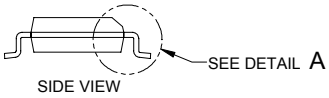
Evaluation Board Bill of Materials

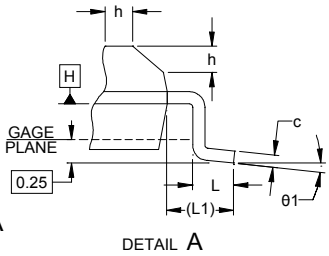
Item	Qty	Reference	Part Number/Value	Manufacturer
1	5	C1,C4,C13,C18,C26	1uf	
2	12	C2,C3,C6,C16,C17,C19,C20, C23,C24,C28,C29,C31	10u,CER	
3	7	C5,C7,C10,C12,C14,C34, C35	820uf,16V	Panasonic
4	1	C9	1u, 16V	
5	1	C11	22nf	
6	3	C15, C21, C22	.1	
7	1	C25	100pf	
8	1	C33	820uf, OS	Sanyo
9	2	D7, D6	LL42	
10	1	J1		
11	2	L2, L1	TTlB1106-708, 700nh	FALCO
12	4	Q1, Q3, Q4, Q5	FDB7030BL	Fairchild
13	1	R1	.005	Dale
14	2	R2, R3	10	
15	5	R5,R8,R9,R13,R99	0	
16	1	R10	100K	
17	2	R11, R20	10k	
18	1	R14	11.5k	
19	1	R17	6.49k	
20	1	R18	1	
21	1	R19	26.7k	
22	1	R30	133	
23	1	R31	100	
24	1	R32	24.3K	
25	1	R33	10.0K	
26	1	S1		
27	2	U3, U1	SC1205	Semtech
28	1	U2	SC2422A	Semtech
29	1	optional	4.7-10 ohm	

Outline Drawing - SO-8







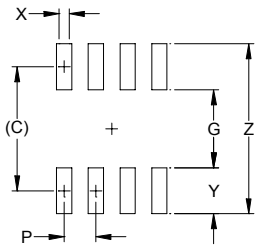


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.004	-	.010	0.10	-	0.25
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.189	.193	.197	4.80	4.90	5.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.04)		
N	8			8		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION AA.

Land Pattern - SO-8



DIM	INCHES	MILLIMETERS
C	(.205)	(5.20)
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 300A.

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