SC1186
Programmable Synchronous DC/DC Converter, Dual LDO Controller

POWER MANAGEMENT

Description

The SC1186 combines a synchronous voltage mode controller with two low-dropout linear regulators providing most of the circuitry necessary to implement three DC/DC converters for powering advanced microprocessors such as Pentium® II & III.

The SC1186 switching section features an integrated 5 bit D/A converter, latched drive output for enhanced noise immunity, pulse by pulse current limiting and logic compatible shutdown. The SC1186 switching section operates at a fixed frequency of 140kHz, providing an optimum compromise between size, efficiency and cost in the intended application areas. The integrated D/A converter provides programmability of output voltage from 2.0V to 3.5V in 100mV increments and 1.30V to 2.05V in 50mV increments with no external components.

The SC1186 linear sections are low dropout regulators with short circuit protection, supplying 1.5V for GTL bus and 2.5V for non-GTL I/O. The Reference voltage is made available for external linear regulators.

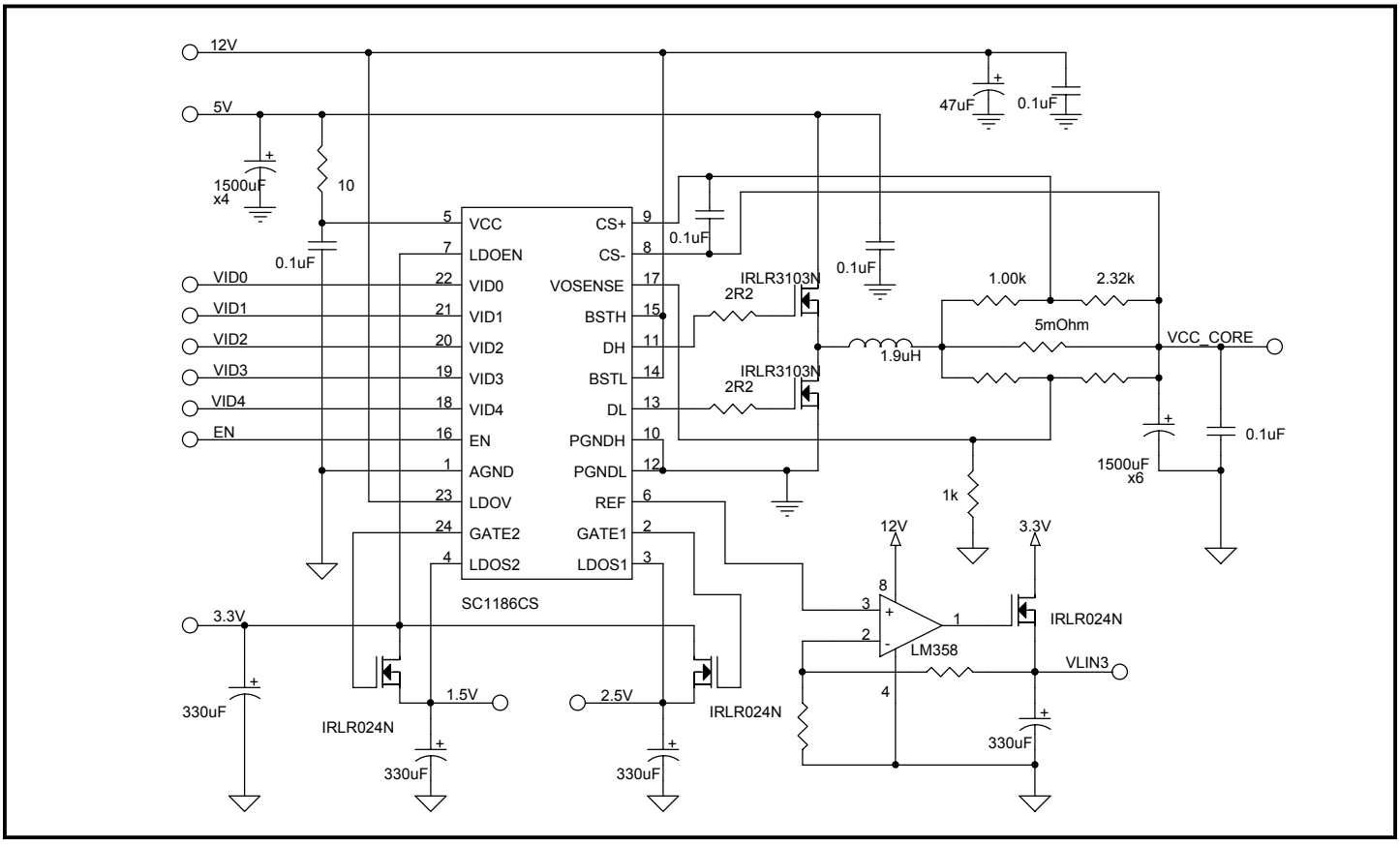
Features

- Synchronous design, enables no heatsink solution
- 95% efficiency (switching section)
- 5 bit DAC for output programmability
- Designed for Intel Pentium® II & III requirements
- 1.5V, 2.5V short circuit protected linear controllers
- 1.265V ± 1.5% Reference available

Applications

- Pentium® II & III microprocessor supplies
- Flexible motherboards
- 1.3V to 3.5V microprocessor supplies
- Programmable triple power supplies

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied. Exposure to Absolute Maximum rated conditions for extended periods of time may affect device reliability.

Parameter	Symbol	Maximum	Units
VCC to AGND	V_{IN}	-0.3 to +7	V
PGNDH, PGNDL to AGND		±1	V
BSTH to PGNDH, BSTL to PGNDL		-0.3 to +15	V
DH to PGNDH, DL to PGNDL (Note2)		-1 to +15	V
Operating Temperature Range	T_A	0 to +70	°C
Junction Temperature Range	T_J	0 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	300	°C
Thermal Resistance Junction to Ambient	θ_{JA}	80	°C/W
Thermal Impedance Junction to Case	θ_{JC}	25	°C/W

Electrical Characteristics

Unless specified: VCC = 4.75V to 5.25V; GND = PGND = 0V; VOSENSE = V_O; 0mV < (CS+-CS-) < 60mV; LDOV = BST = 11.4V to 12.6V; T_A = 0 to 70°C

Parameter	Conditions	Min	Typ	Max	Units
Switching Section					
Output Voltage	I_O = 2A in Application Circuit	See Output Voltage Table			
Supply Voltage	VCC	4.5		7	V
Supply Current	VCC = 5.0V		8	15	mA
Load Regulation	I_O = 0.8A to 15A		1		%
Line Regulation			±0.5		%
Current Limit Voltage		60	70	85	mV
Oscillator Frequency		120	140	160	kHz
Oscillator Max Duty Cycle		90	95		%
Peak DH Sink/Source Current	BSTH - DH = 4.5V, DH- PGNDH = 3.3V DH- PGNDH = 1.5V	1 100			A mA
Peak DL Sink/Source Current	BSTL - DL = 4.5V, DL - PGNDL= 3.3V DL- PGNDH = 1.5V	1 100			A mA
Gain (A_{OL})	VOSENSE to V_O		35		dB
VID Source Current	VIDx < 2.4V	1	10		uA
VID Leakage	VIDx = 5V			10	uA
Power good threshold voltage		88		112	%
Dead Time		40	100		ns

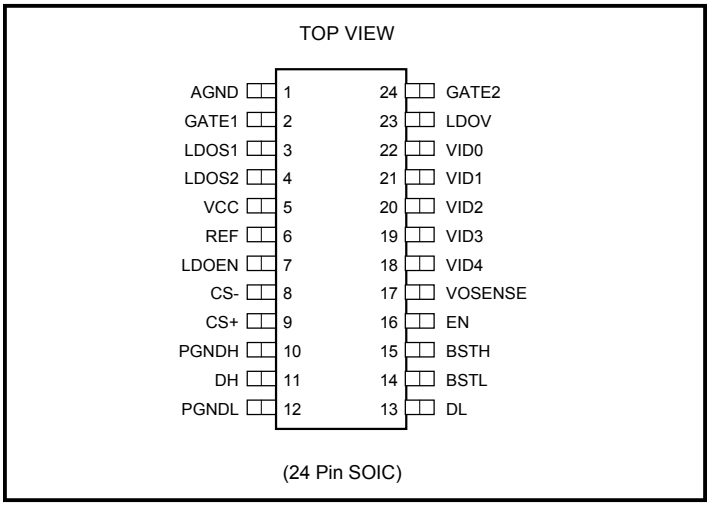
Electrical Characteristics (Cont.)

Unless specified: VCC = 4.75V to 5.25V; GND = PGND = 0V; VOSENSE = V_O; 0mV < (CS+-CS-) < 60mV; LDOV = BST = 11.4V to 12.6V; T_A = 0 to 70°C

Parameter	Conditions	Min	Typ	Max	Units
Linear Sections					
Quiescent Current	LDOV = 12V			5	mA
Output Voltage LDO1		2.493	2.525	2.556	V
Output Voltage LDO2		1.496	1.515	1.534	V
Reference Voltage	Iref < 100uA	1.246	1.265	1.284	V
Gain (A_{OL})	LDOS (1,2) to GATE (1,2)		90		dB
Load Regulation	I_O = 0 to 8A			0.3	%
Line Regulation				0.3	%
Output Impedance	VGATE = 6.5V		1	1.5	kΩ
LDOV Undervoltage Lockout		6.5	8.0	10	V
LDOEN Threshold		1.3		1.9	V
LDOEN Sink Current	LDOEN = 3.3V LDOEN = 0V		0.01 -200	1.0 -300	µA µA
Overcurrent Trip Voltage	% of Vo set point	20	40	60	%
Power-up Output Short Circuit Immunity		1	5	60	ms
Output Short Circuit Glitch Immunity		0.5	4	20	ms
Gate Pulldown Impedance	GATE (1,2) -AGND; VCC+BST=0V	80	300	750	kΩ
VOSENSE Impedance		10			kΩ

Note:
(1) This device is ESD sensitive. Use of standard ESD handling precautions is required.
(2) See Gate Resistor Selection recomendations.

Pin Configuration



Ordering Information

Device (1)	Package(1)	Linear Voltage	Temp Range (T_J)
SC1186CSW.TR	SO-24	1.5V/2.5V	0° to 125°C
SC1186CSWTRT(2)			

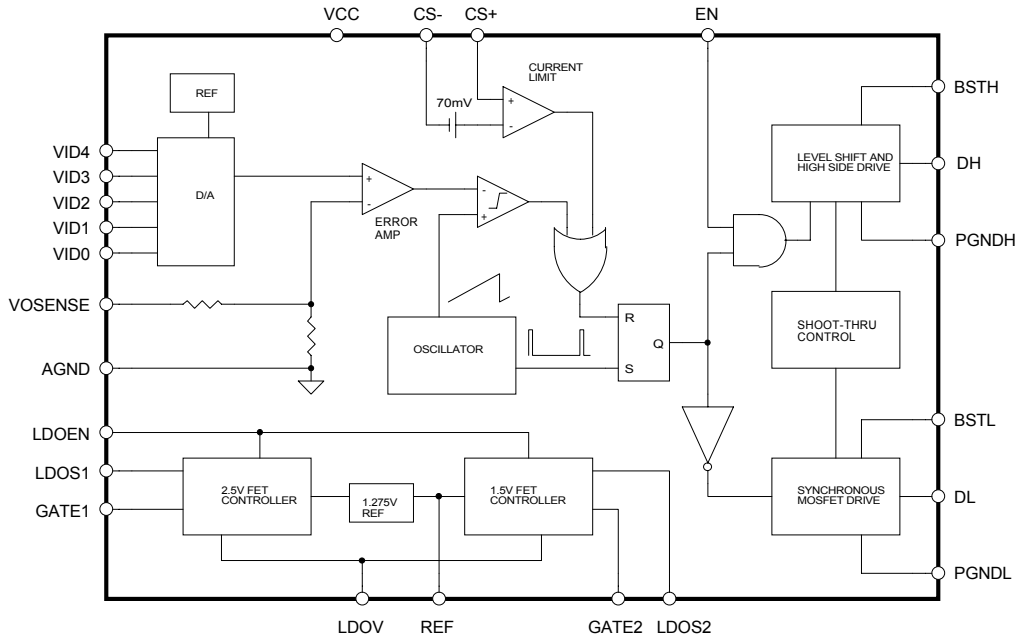
Notes:
(1) Only available in tape and reel packaging. A reel contains 1000 devices.
(2) Lead free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	AGND	Small Signal Analog and Digital Ground
2	GATE1	Gate Drive Output LDO1
3	LDOS1	Sense Input for LDO1
4	LDOS2	Sense Input for LDO2
5	VCC	Input Voltage
6	REF	Buffered Reference Voltage output
7	LDOEN	LDO Supply Monitor.
8	CS-	Current Sense Input (negative)
9	CS+	Current Sense Input (positive)
10	PGNDH	Power Ground for High Side Switch
11	DH	High Side Driver Output
12	PGNDL	Power Ground for Low Side Switch
13	DL	Low Side Driver Output
14	BSTL	Supply for Low Side Driver
15	BSTH	Supply for High Side Driver
16	EN (1)	Logic low shuts down the converter, High or open for normal operation
17	VOSENSE	Top end of internal feedback chain.
18	VID4 (1)	Programming Input (MSB)
19	VID3 (1)	Programming Input
20	VID2 (1)	Programming Input
21	VID1 (1)	Programming Input
22	VID0 (1)	Programming Input (LSB)
23	LDOV	+12V for LDO section
24	GATE2	Gate Drive Output LDO2

Note:
(1) All logic level inputs and outputs are open collector TTL compatible.

Block Diagram



Applications Information - Output Voltage Table

Unless specified: 4.75V < VCC < 5.25V; GND = PGND = 0V; VOSENSE = V_O; 0mV < (CS+-CS-) < 60mV; = 0°C < T_j < 85°C

Parameter	Conditions	Vid 43210	Min	Typ	Max	Units
Output Voltage (1)	I_O = 2A in Application circuit (Figure 1)	01111	1.277	1.300	1.323	V
		01110	1.326	1.350	1.374	
		01101	1.375	1.400	1.425	
		01100	1.424	1.450	1.476	
		01011	1.478	1.500	1.523	
		01010	1.527	1.550	1.573	
		01001	1.576	1.600	1.624	
		01000	1.625	1.650	1.675	
		00111	1.675	1.700	1.726	
		00110	1.724	1.750	1.776	
		00101	1.782	1.800	1.818	
		00100	1.832	1.850	1.869	
		00011	1.881	1.900	1.919	
		00010	1.931	1.950	1.970	
		00001	1.980	2.000	2.020	
		00000	2.030	2.050	2.071	
		11111	1.970	2.000	2.030	
		11110	2.069	2.100	2.132	
		11101	2.167	2.200	2.233	
		11100	2.266	2.300	2.335	
		11011	2.364	2.400	2.436	
		11010	2.463	2.500	2.538	
		11001	2.561	2.600	2.639	
		11000	2.660	2.700	2.741	
		10111	2.758	2.800	2.842	
		10110	2.842	2.900	2.958	
		10101	2.940	3.000	3.060	
		10100	3.038	3.100	3.162	
		10011	3.136	3.200	3.264	
		10010	3.234	3.300	3.366	
		10001	3.332	3.400	3.468	
		10000	3.430	3.500	3.570	

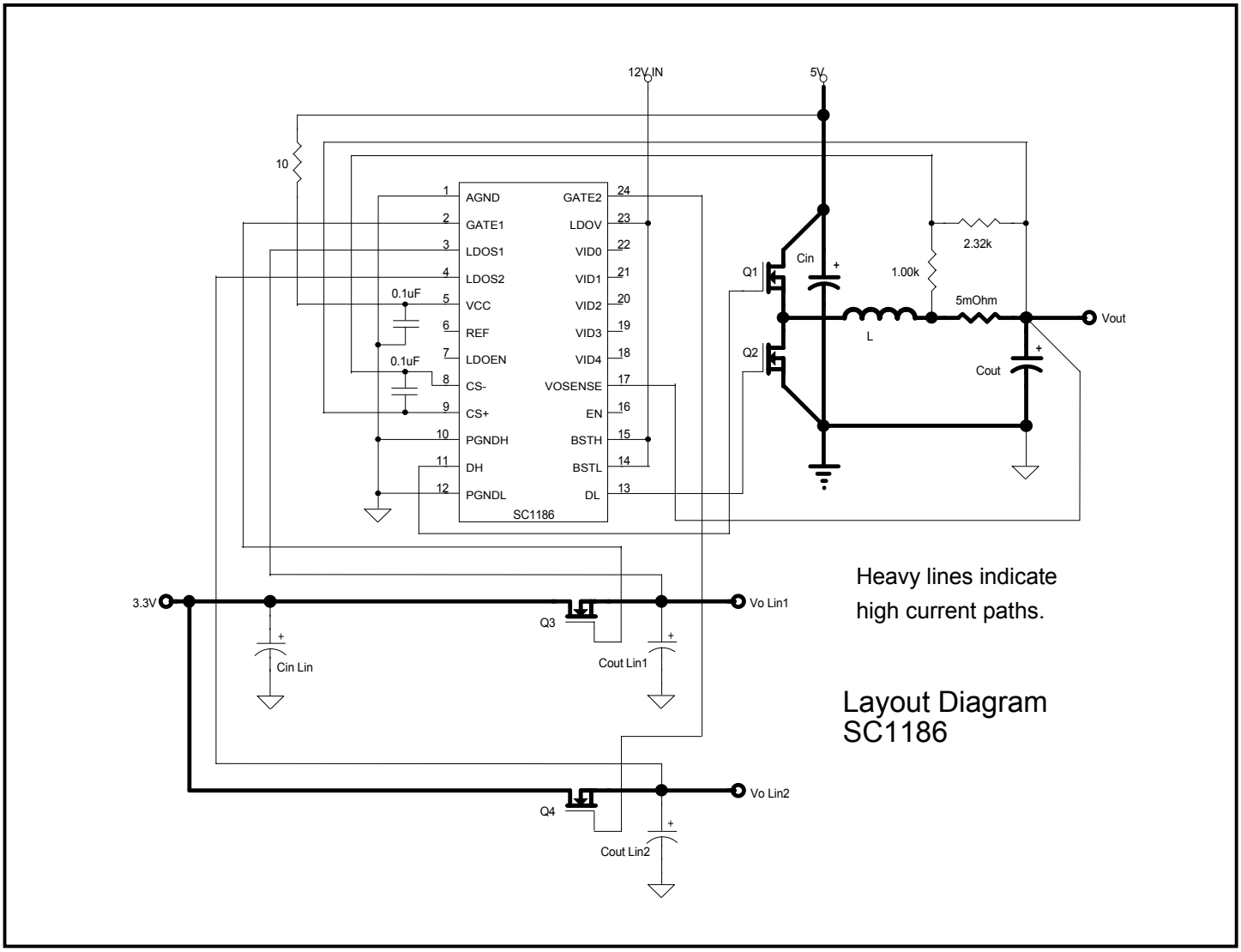
Layout Guidelines

Careful attention to layout requirements are necessary for successful implementation of the SC1186 PWM controller. High currents switching at 140kHz are present in the application and their effect on ground plane voltage differentials must be understood and minimized.

1). The high power parts of the circuit should be laid out first. A ground plane should be used, the number and position of ground plane interruptions should be such as to not unnecessarily compromise ground plane integrity. Isolated or semi-isolated areas of the ground plane may be deliberately introduced to constrain ground currents to particular areas, for example the input capacitor and bottom FET ground.

2). The loop formed by the Input Capacitor(s) (Cin), the Top FET (Q1) and the Bottom FET (Q2) must be kept as small as possible. This loop contains all the high current, fast transition switching. Connections should be as wide and as short as possible to minimize loop inductance. Minimizing this loop area will a) reduce EMI, b) lower ground injection currents, resulting in electrically “cleaner” grounds for the rest of the system and c) minimize source ringing, resulting in more reliable gate switching signals.

3). The connection between the junction of Q1, Q2 and the output inductor should be a wide trace or copper region. It should be as short as practical. Since this connection has fast voltage transitions, keeping this connection short will minimize EMI. The connection between the output inductor and the sense resistor should be a wide trace or copper area, there are no fast voltage or current transitions in this connection and length is not so important, however adding unnecessary impedance will reduce efficiency.



Layout Guidelines (Cont.)

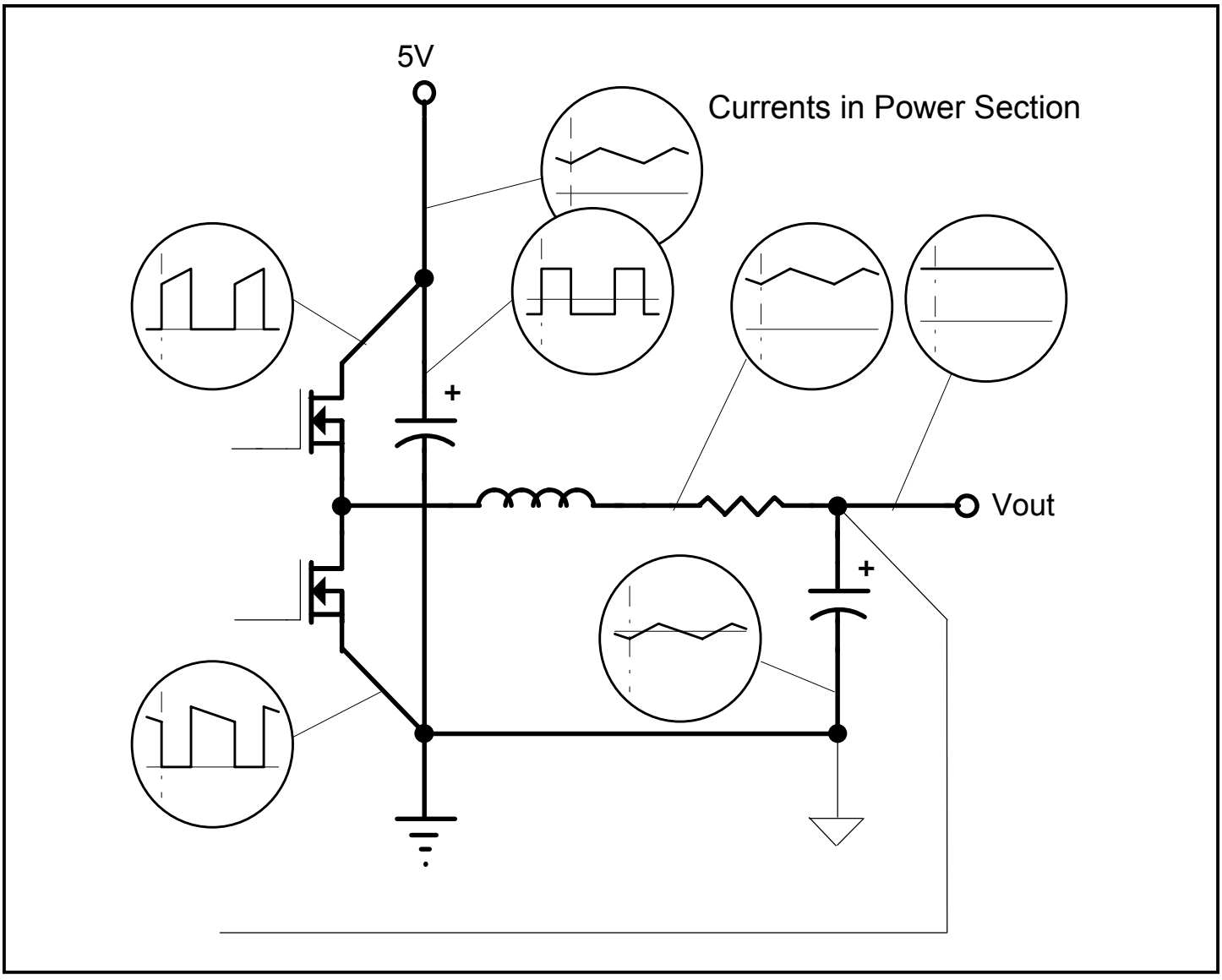
4) The Output Capacitor(s) (Cout) should be located as close to the load as possible, fast transient load currents are supplied by Cout only, and connections between Cout and the load must be short, wide copper areas to minimize inductance and resistance.

5) The SC1186 is best placed over a quiet ground plane area, avoid pulse currents in the Cin, Q1, Q2 loop flowing in this area. PGNDH and PGNDL should be returned to the ground plane close to the package. The AGND pin should be connected to the ground side of (one of) the output capacitor(s). If this is not possible, the AGND pin may be connected to the ground path between the Output Capacitor(s) and the Cin, Q1, Q2 loop. Under no circumstances should AGND be returned to a ground inside the Cin, Q1, Q2 loop.

6) Vcc for the SC1186 should be supplied from the 5V supply through a 10Ω resistor, the Vcc pin should be decoupled directly to AGND by a 0.1µF ceramic capacitor, trace lengths should be as short as possible.

7) The Current Sense resistor and the divider across it should form as small a loop as possible, the traces running back to CS+ and CS- on the SC1186 should run parallel and close to each other. The 0.1µF capacitor should be mounted as close to the CS+ and CS- pins as possible.

8) Ideally, the grounds for the two LDO sections should be returned to the ground side of (one of) the output capacitor(s).



Component Selection

SWITCHING SECTION

OUTPUT CAPACITORS - Selection begins with the most critical component. Because of fast transient load current requirements in modern microprocessor core supplies, the output capacitors must supply all transient load current requirements until the current in the output inductor ramps up to the new level. Output capacitor ESR is therefore one of the most important criteria. The maximum ESR can be simply calculated from:

$$R_{ESR} \leq \frac{V_t}{I_t}$$

Where

V_t = Maximum transient voltage excursion

I_t = Transient current step

For example, to meet a 100mV transient limit with a 10A load step, the output capacitor ESR must be less than 10mΩ. To meet this kind of ESR level, there are three available capacitor technologies.

Technology	Each Cap.		Qty. Rqd.	Total	
	C (µF)	ESR (mΩ)		C (µF)	ESR (mΩ)
Low ESR Tantalum	330	60	6	2000	10
OS-CON	330	25	3	990	8.3
Low ESR Aluminum	1500	44	5	7500	8.3

The choice of which to use is simply a cost/performance issue, with Low ESR Aluminum being the cheapest, but taking up the most space.

INDUCTOR - Having decided on a suitable type and value of output capacitor, the maximum allowable value of inductor can be calculated. Too large an inductor will produce a slow current ramp rate and will cause the output capacitor to supply more of the transient load current for longer - leading to an output voltage sag below the ESR excursion calculated above.

The maximum inductor value may be calculated from:

$$L \leq \frac{R_{ESR}\, C}{I_t} \cdot V_A$$

where V_A is the lesser of V_O or $(V_{IN} - V_O)$

The calculated maximum inductor value assumes 100% and 0% duty cycle capability, so some allowance must be made. Choosing an inductor value of 50 to 75% of the calculated maximum will guarantee that the inductor current will ramp fast enough to reduce the voltage dropped across the ESR at a faster rate than the capacitor sags, hence ensuring a good recovery from transient with no additional excursions.

We must also be concerned with ripple current in the output inductor and a general rule of thumb has been to allow 10% of maximum output current as ripple current. Note that most of the output voltage ripple is produced by the inductor ripple current flowing in the output capacitor ESR. Ripple current can be calculated from:

$$I_{L_{RIPPLE}} = \frac{V_{IN}}{4 \cdot L \cdot f_{OSC}}$$

Ripple current allowance will define the minimum permitted inductor value.

POWER FETS - The FETs are chosen based on several criteria, with probably the most important being power dissipation and power handling capability.

TOP FET - The power dissipation in the top FET is a combination of conduction losses, switching losses and bottom FET body diode recovery losses.

a) Conduction losses are simply calculated as:

$$P_{COND} = I_O^2 \cdot R_{DS(on)} \cdot \delta$$

where

δ = duty cycle $\approx \frac{V_O}{V_{IN}}$

b) Switching losses can be estimated by assuming a switching time, if we assume 100ns then:

$$P_{SW} = I_O \cdot V_{IN} \cdot 10^{-2}$$

or more generally,

$$P_{SW} = \frac{I_O \cdot V_{IN} \cdot (t_r + t_f) \cdot f_{OSC}}{4}$$

c) Body diode recovery losses are more difficult to estimate, but to a first approximation, it is reasonable to assume that the stored charge on the bottom FET body diode will be moved through the top FET as it starts to turn on. The resulting power dissipation in the top FET will be:

$$P_{RR} = Q_{RR} \cdot V_{IN} \cdot f_{OSC}$$

Component Selection (Cont.)

To a first order approximation, it is convenient to only consider conduction losses to determine FET suitability. For a 5V in; 2.8V out at 14.2A requirement, typical FET losses would be:
Using 1.5X Room temp $R_{DS(ON)}$ to allow for temperature rise.

FET type	$R_{DS(on)}$ (mΩ)	P_D (W)	Package
IRL34025	15	1.69	D²Pak
IRL2203	10.5	1.19	D²Pak
Si4410	20	2.26	S0-8

BOTTOM FET - Bottom FET losses are almost entirely due to conduction. The body diode is forced into conduction at the beginning and end of the bottom switch conduction period, so when the FET turns on and off, there is very little voltage across it, resulting in low switching losses. Conduction losses for the FET can be determined by:

$$P_{COND} = I_O^2 \cdot R_{DS(on)} \cdot (1-\delta)$$

For the example above:

FET type	$R_{DS(on)}$ (mΩ)	P_D (W)	Package
IRL34025	15	1.33	D²Pak
IRL2203	10.5	0.93	D²Pak
Si4410	20	1.77	S0-8

Each of the package types has a characteristic thermal impedance. For the surface mount packages on double sided FR4, 2 oz printed circuit board material, thermal impedances of 40°C/W for the D²PAK and 80°C/W for the SO-8 are readily achievable. The corresponding temperature rise is detailed below:

	Temperature Rise (°C)	
FET type	Top FET	Bottom FET
IRL34025	67.6	53.2
IRL2203	47.6	37.2
Si4410	180.8	141.6

It is apparent that single SO-8 Si4410 are not adequate for this application, but by using parallel pairs in each position, power dissipation will be approximately halved and temperature rise reduced by a factor of 4.

INPUT CAPACITORS - since the RMS ripple current in the input capacitors may be as high as 50% of the output current, suitable capacitors must be chosen accordingly. Also, during fast load transients, there may be restrictions on input di/dt. These restrictions require useable energy storage within the converter circuitry, either as extra output capacitance or, more usually, additional input capacitors. Choosing low ESR input capacitors will help maximize ripple rating for a given size.

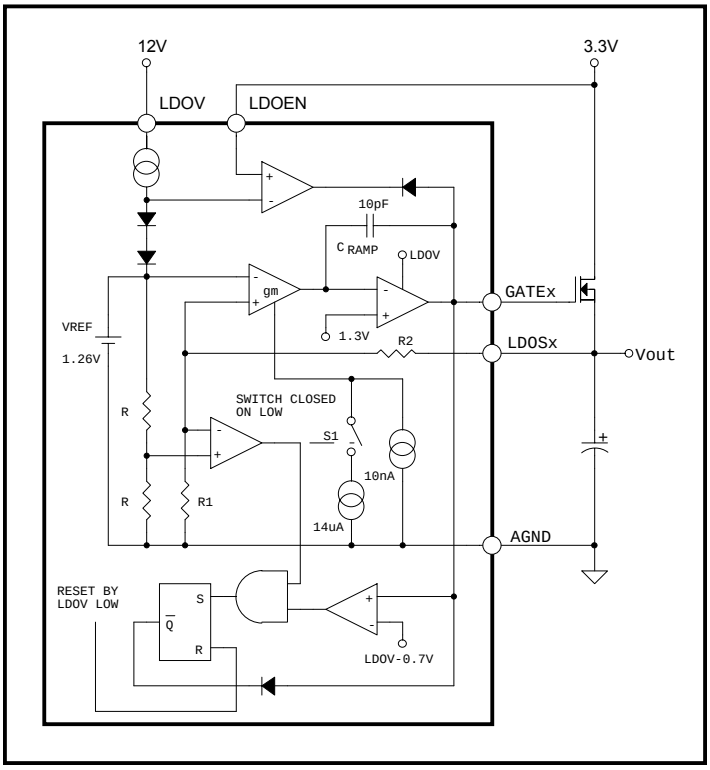
GATE RESISTOR SELECTION - The gate resistors for the top and bottom switching FETs limit the peak gate current and hence control the transition time. It is important to control the off time transition of the top FET, it should be fast to limit switching losses, but not so fast as to cause excessive phase node oscillation below ground as this can lead to current injection in the IC substrate and erratic behaviour or latchup. The actual value should be determined in the application, with the final layout and FETs.

SHORT CIRCUIT PROTECTION - LINEARS

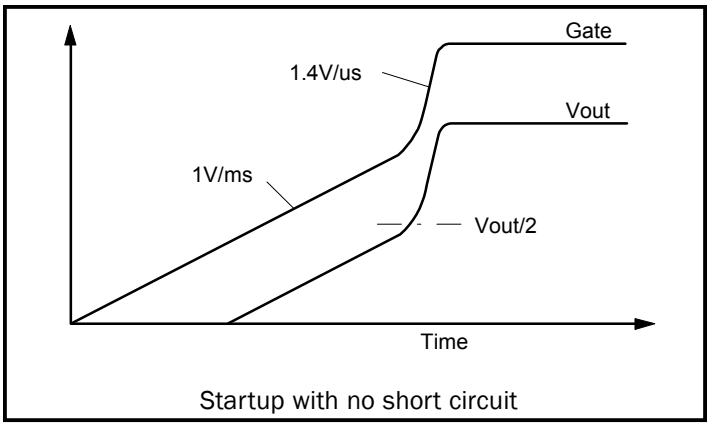
The Short circuit feature on the linear controllers is implemented by using the Rds(on) of the FETs. As output current increases, the regulation loop maintains the output voltage by turning the FET on more and more. Eventually, as the Rds(on) limit is reached, the FET will be unably to turn on more fully, and output voltage will start to fall. When the output voltage falls to approximately 40% of nominal, the LDO controller is latched off, setting output voltage to 0. Power must be cycled to reset the latch.
To prevent false latching due to capacitor inrush currents or low supply rails, the current limit latch is initially disabled. It is enabled at a preset time (nominally 2ms) after both the LDOV and LDOEN pins rise above their lockout points.
To be most effective, the linear FET Rds(on) should not be selected artificially low, the FET should be chosen so that, at maximum required current, it is almost fully turned on. If, for example, a linear supply of 1.5V at 4A is required from a 3.3V ± 5% rail, max allowable Rds(on) would be.
Rds(on)max = (0.95*3.3-1.5)/4 » 400mΩ
To allow for temperature effects 200mΩ would be a suitable room temperature maximum, allowing a peak short circuit current of approximately 15A for a short time before shutdown.

Theory of Operation (Linear OCP)

The Linear controllers in the SC1186 have built in Overcurrent Protection (OCP). An overcurrent is assumed to have occured when the external FET is turned fully on and the output currrent is $R_{DS(ON)}$ limited, this is detected by the gate voltage going very high while the output voltage is below approximately 40% of it's setpoint. To allow for capacitor charging and very short overcurrent durations, the gate voltage is ramped very slowly upwards whenever the output voltage is below the OCP threshold. To guarantee that the LDO output voltage is capable of reaching it's setpoint, the gate drive is disabled until both LDOV Undervoltage Lockout (UVLO) and LDOEN Threshold values are exceeded, ensuring that there is sufficient gate drive capability and sufficient LDO input voltage capability. A block diagram of one LDO controller is shown below.

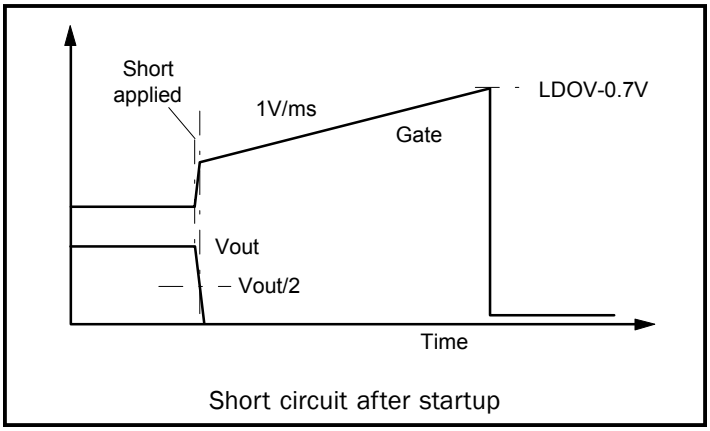


During a normal start-up, once LDOV and LDOEN have reached their thresholds, the GATEx pin is released and C_{RAMP} is charged by 10nA causing the GATEx voltage to ramp at 10nA/10pF = 1V/ms. Once the GATEx output has ramped to the external FET threshold, Vout starts to ramp up, following GATEx. When Vout reaches the OCP threshold, approximately 40% of setpoint, switch S1 is closed and GATEx ramps up at a much faster rate, followed by Vout, until Vout reaches setpoint and the loop settles into steady state regulation.



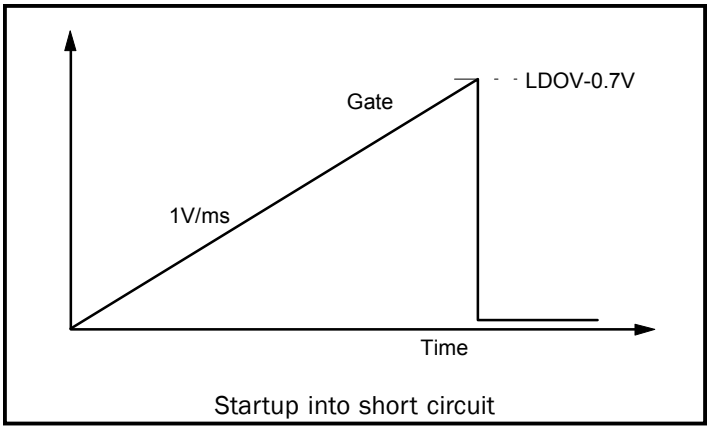
Startup with no short circuit

If at some later time, a short circuit is applied to the output, the GATEx voltage will ramp up quickly as Vout falls to try and maintain regulation. Once Vout has fallen to the OCP threshold, switch S1 will open and the gate will continue ramping at the 1V/ms rate. If the short is not removed before the GATEx output reaches approximately LDOV - 0.7V, the GATEx pin will be latched low, disabling the LDO



Short circuit after startup

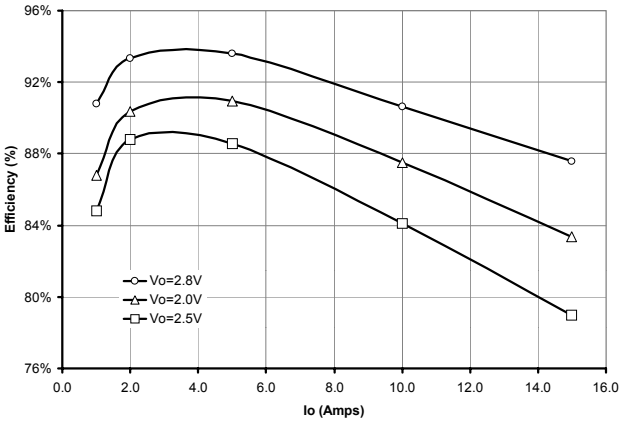
If the LDO tries to start into a short, the gate ramps at the 1V/ms rate to LDOV - 0.7V, where the GATEx pin will be latched low.



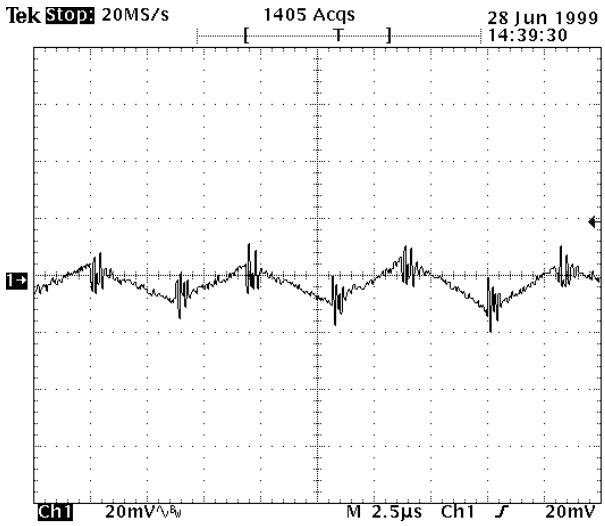
Startup into short circuit

Typical Characteristics

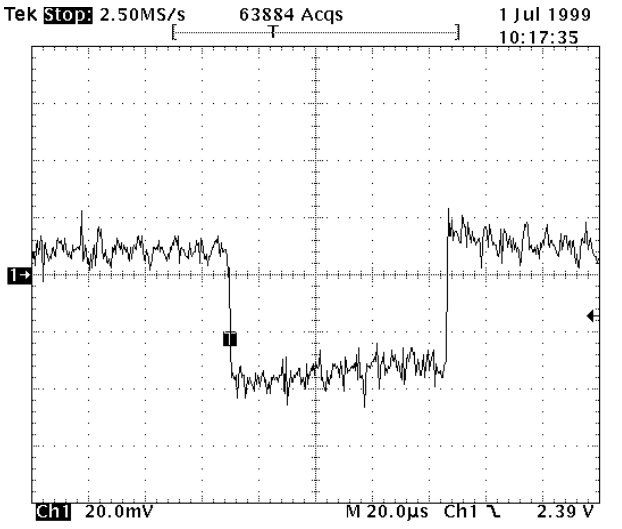
Typical Efficiency (Switching section)



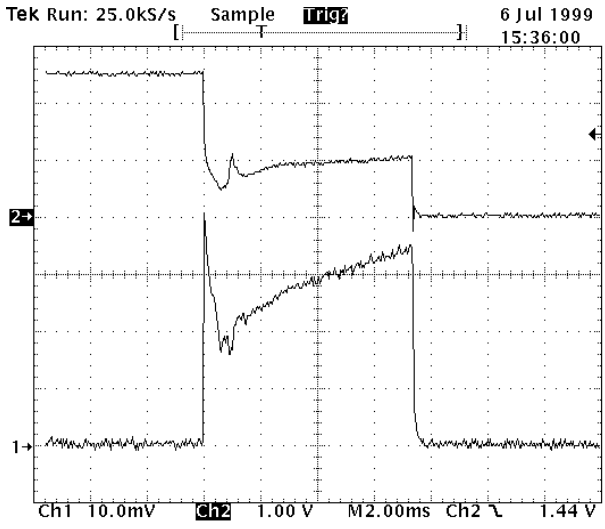
Typical Ripple, Vo=2.0V, Io=10A



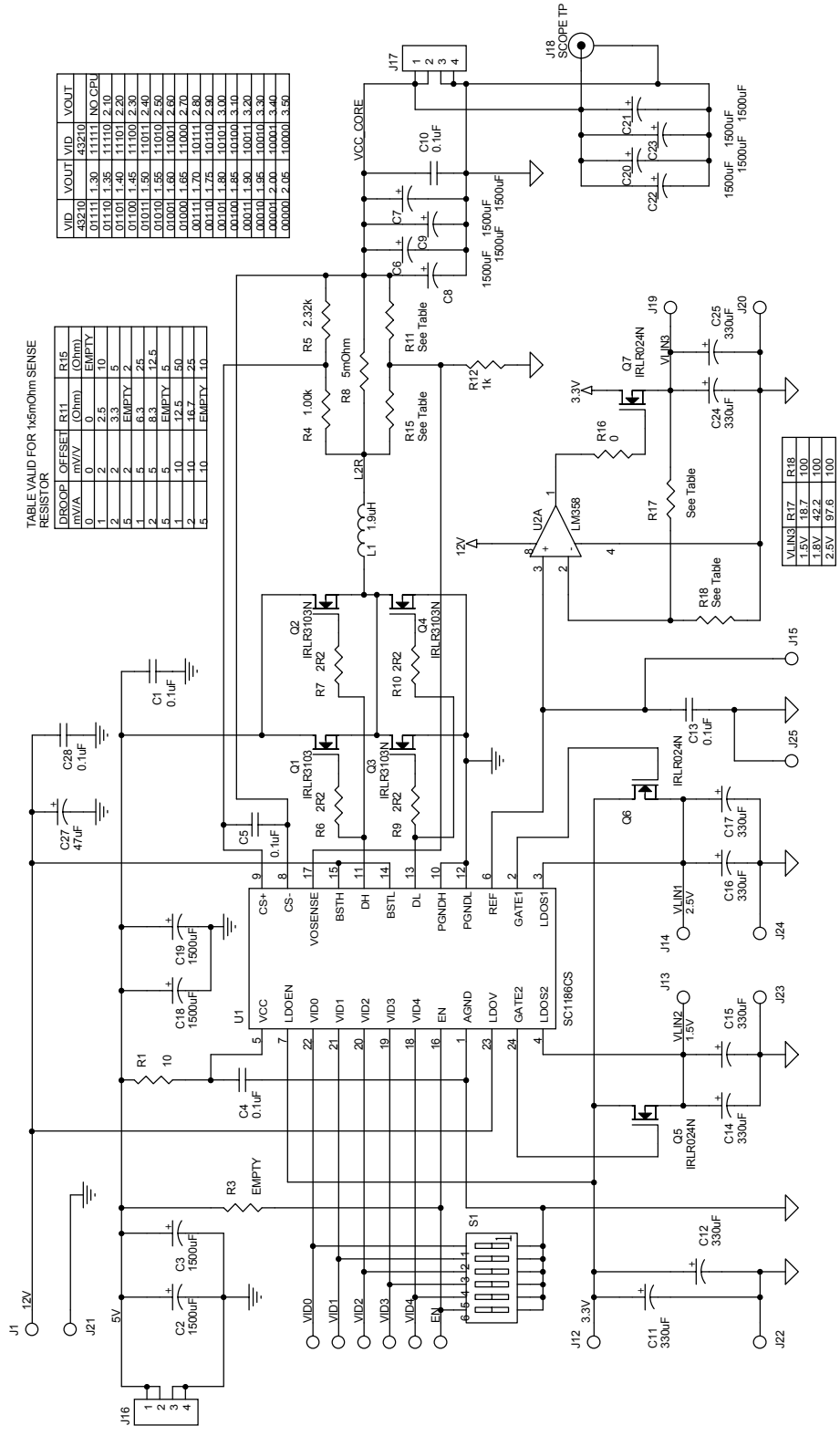
Transient Response Vo=2.4V, Io=300mA to 15A



2.5V Linear Short circuit output response



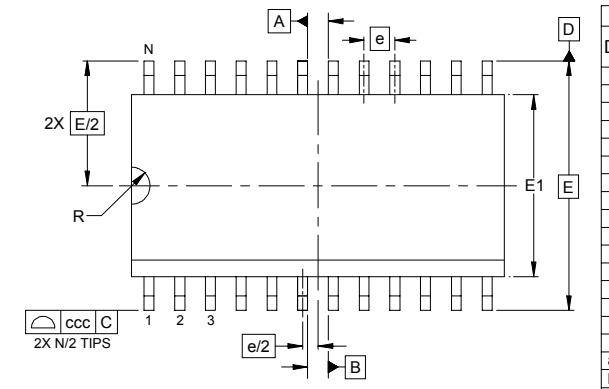
Evaluation Board Schematic



Evaluation Board Bill of Materials

Item	Qty.	Reference	Value	Notes
1	6	C1, C4, C5, C10, C13, C28	0.1uF	
2	12	C2, C3, C6, C7, C8, C9, C18, C19, C20, C21, C22, C23	1500uF	Low ESR Sanyo MV-GX or equivalent
3	8	C11, C12, C14, C15, C16, C17, C24, C25	330uF	
4	1	C27	47uF	
5	1	L1	1.9uH	
6	3	Q1, Q2, Q3, Q4	IRLR3103N	
7	3	Q5, Q6, Q7	IRLR024N	
8	1	R1	10	
9	1	R3	EMPTY	
10	1	R4	1.00k	1%
11	1	R5	2.32k	1%
12	4	R6, R7, R9, R10	2R2	
13	1	R8	5mOhm	IRC OAR1
14	2	R15, R11	See Table 2	
15	1	R12	1k	
16	1	R16	0	
17	2	R17, R18	See Table	
18	1	U1	SC1186CS	SEMTECH
19	1	U2	LM358	

Outline Drawing - SO-24

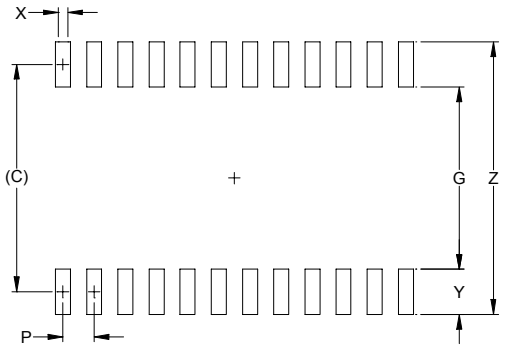


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.093	-	.104	2.35	-	2.65
A1	.004	-	.012	0.10	-	0.30
A2	.081	-	.100	2.05	-	2.55
b	.012	-	.020	0.31	-	0.51
c	.008	-	.013	0.20	-	0.33
D	.602	.606	.610	15.30	15.40	15.50
E1	.291	.295	.299	7.40	7.50	7.60
E	.406 BSC			10.30 BSC		
e	.050 BSC			1.27 BSC		
h	.010	-	.030	0.25	-	0.75
J	.020	-	.030	0.50	-	0.75
L	.016	-	.041	0.40	-	1.04
L1	(.041)			(1.04)		
N	24			24		
R	.024	-	.035	0.60	-	0.90
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.013			0.33		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-013, VARIATION AD.

Outline Drawing - SO-24



DIM	INCHES	MILLIMETERS
C	(.362)	(9.20)
G	.276	7.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.449	11.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 307A.

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