SC412A
Synchronous Buck Controller

Description

The SC412A is a versatile, constant on-time synchronous buck, pseudo fixed-frequency, PWM controller intended for notebook computers and other battery operated portable devices. The SC412A contains all the features needed to provide cost-effective control of switch-mode power outputs.

The output voltage is programmable from 0.75 to 5.25 volts using external resistors. Switching frequency is internally preset to 325kHz. Additional features cycle-by-cycle current limit, voltage soft-start, under-voltage protection, programmable over-current protection, soft shutdown, automatic power save and non-overlapping gate drive. The SC412A also provides an enable input and a power good output.

The constant on-time topology provides fast, dynamic response. The excellent transient response means that SC412A based solutions require less output capacitance than competing fixed-frequency converters. Switching frequency is constant until a step in load or line voltage occurs, at which time the pulse density and frequency will increase or decrease to counter the change in output voltage. After the transient event, the controller frequency returns to steady state operation. At light loads, the automatic power save mode reduces the switching frequency for improved efficiency.

Features

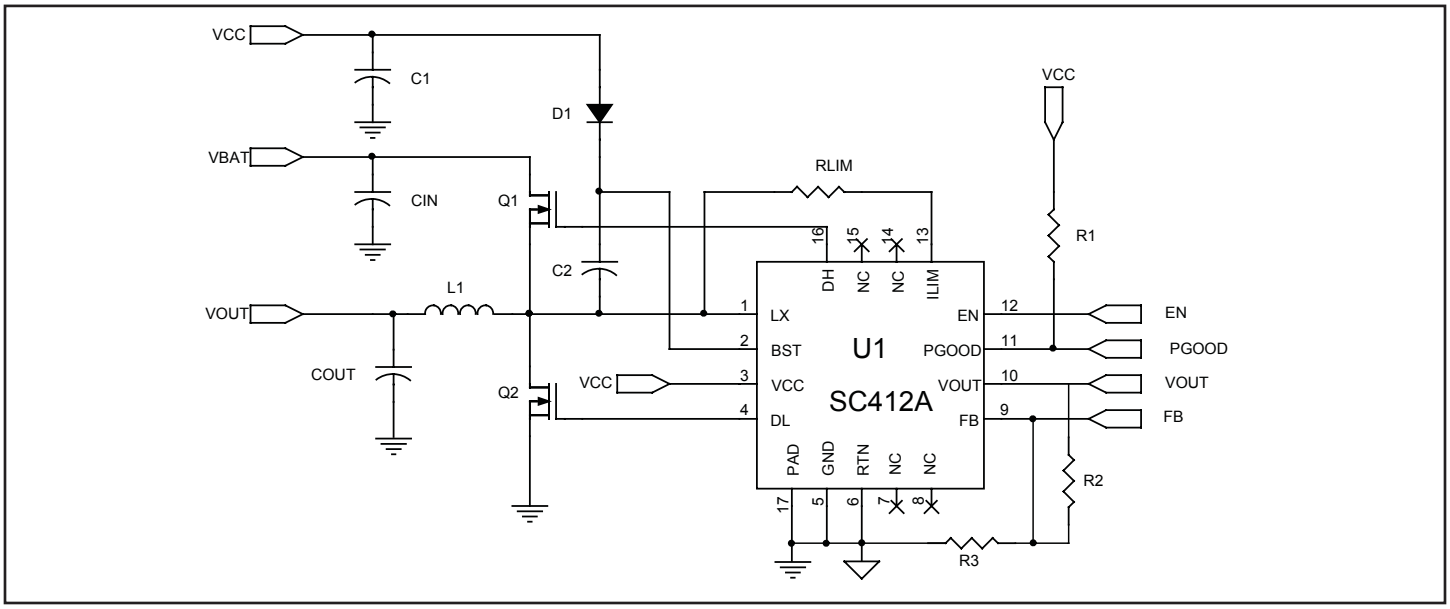
- V_{BAT} Range 3V to 25V
- Soft-Shutoff at Output
- Current Sense Using Low-Side $R_{DS(ON)}$ or Resistor Sensing with Adjustable Cycle-by-Cycle Current Limit
- Fixed-Frequency 325kHz
- Constant On-Time for Fast Dynamic Response and Reduced Output Capacitance
- Automatic Smart Power Save†
- Internal Soft-Start
- Over-Voltage/Under-Voltage Fault Protection
- Power Good Output
- 1µA Typical Shutdown Current
- Tiny 3x3mm, 16 Pin MLP, Lead-free Package
- Low External Part Count
- Industrial Temperature Range
- 1% Internal Reference
- 1A/3A Non-Overlapping Gate Drive with SmartDrive™
- High Efficiency > 90%
- Fully WEEE and RoHS Compliant

†Patent pending

Applications

- Notebook and Sub-Notebook Voltage Controllers
- Tablet PCs
- Embedded Applications

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied. Exposure to Absolute Maximum rated conditions for extended periods of time may affect device reliability.

Parameter	Symbol	Min	Max	Units
DH, BST to GND (DC) DH, BST to GND (transient - 100nsec max)		-0.3 -2.0	+30 +33	V
DL to GND (DC) DL to GND (transient - 100nsec max)		-0.3 -2.0	+6.0 +6.0	V
LX to GND (DC) LX to GND (transient - 100nsec max)		-0.3 -2.0	+25 +28	V
BST to LX		-0.3	+6.0	V
RTN to GND		-0.3	+0.3	V
VCC to RTN		-0.3	+6.0	V
EN, FB, ILIM, PGOOD, VCC, VOUT to RTN		-0.3	VCC + 0.3	V
Operating Junction Temperature Range	T_J	-40	+125	°C
Storage Temperature Range	T_{STG}	-60	+150	°C
Thermal Resistance, Junction to Ambient(1)	θ_{JA}	45		°C/Watt
Peak IR Reflow Temperature, 10-40 Second	T_{PKG}		+260	°C
ESD Rating (Human Body Model)		2		kV

Note:
(1) Calculated from package in still air, mounted 3" to 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Test Conditions: V_{BAT} = 15V, V_{OUT} = 1.5V, T_A = 25°C, 0.1% resistor dividers; V_{CC} = 5.0V, unless otherwise noted.

Parameter	Conditions	25°C			-40° to 85°C		Units
		Min	Typ	Max	Min	Max	
Input Supplies							
VBAT Input Voltage		3.0		25			V
VCC Shutdown Current	EN = 0V		1			5	µA
VCC Operating Current	FB > REF		500			1000	µA
Controller							
FB On-Time Threshold			0.75		0.7425	0.7575	V
Regulation							
Line Regulation Error	Typical Application Circuit		0.04				%/V
Load Regulation Error	Typical Application Circuit		0.3				%

Electrical Characteristics *(continued)*

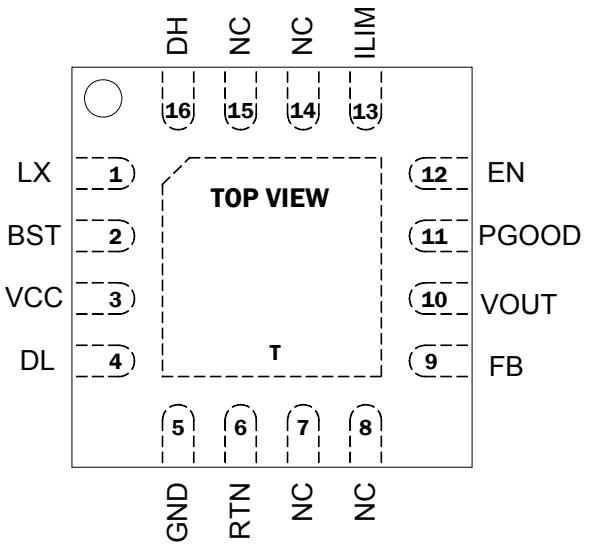
Parameter	Conditions	25°C			-40° to 85°C		Units
		Min	Typ	Max	Min	Max	
Timing							
On-Time	Continuous Mode Operation V_{OUT} = 1.1V		250		225	275	ns
Minimum On-Time			100				ns
Minimum Off-Time			350				
Maximum Duty Cycle	$V_{BAT} \leq V_{OUT}$ +0.2 V_{OUT} < On-Time Threshold		85		80		%
Soft-Start							
Soft-Start Time	I_{OUT} = ILIM/2		1000				µs
Analog Inputs/Outputs							
VOUT Input Resistance			500				kΩ
Current Sense							
Zero-Crossing Detector Threshold	LX - GND		0		-7	+7	mV
Power Good							
Power Good Threshold	1% HysteresisTypical		-12%		-9%	-15%	%
Threshold Delay Time(1)			5				µs
Leakage						1	µA
Fault Protection							
ILIM Source Current			10		9	11	µA
ILIM Comparator Offset			0		-10	+10	mV
Current Limit (Negative)	LX - GND		80		60	100	mV
Output Under-Voltage Fault	FB with Respect to REF		-30		-35	-25	%
Steady-State Over-Voltage Fault	FB with Respect to REF		20		+17	+23	%
Over-Voltage Fault Delay(1)	FB Forced 50mV Above Over-Voltage Fault Threshold		5				µs
VCCA Under-Voltage (UVLO)	Conditions = Falling Edge (Hysteresis 100mV)		4		3.7	4.35	V
Over-Temperature Shutdown(1)			160				°C
Logic Inputs/Outputs							
Logic Input Hgh Voltage	EN				1.2		V
Logic Input Low Voltage	EN					0.4	V

Electrical Characteristics *(continued)*

Parameter	Conditions	25°C			-40° to 85°C		Units
		Min	Typ	Max	Min	Max	
Logic Inputs/Outputs *(continued)*							
EN Input Bias Current	EN = V_{CC} or R_{TN}				-1	+1	µA
FB Input Bias Current	FB = V_{CC} or R_{TN}				-1	+1	µA
Power Good Output Low Voltage	R_{PWRGD} = 10kΩ to V_{CC}					0.4	V
Gate Drivers							
Shoot-Through Protection Delay(1)	DH or DL Rising		30				ns
DL Pull-Down Resistance	DL Low		0.8			1.6	Ω
DL Sink Current	V_{DL} = 2.5V		3.1				A
DL Pull-Up Resistance	DL High		2			4	Ω
DL Source Current	V_{DL} = 2.5V		1.3				A
DH Pull-Down Resistance	DH Low, BST - LX = 5V		2			4	Ω
DH Pull-Up Resistance(2)	DH High, BST - LX = 5V		2			4	Ω
DH Sink/Source Current	V_{DH} = 2.5V		1.3				A

Notes:
(1) Guaranteed by design.
(2) Semtech's SmartDriver™ FET drive first pulls DH high with a pull-up resistance of 10Ω (typical) until LX = 1.5V (typical). At this point, an additional pull-up device is activated, reducing the resistance to 2Ω (typical). This negates the need for an external gate or boost resistor.

Pin Configuration



MLPQ16: 3X3 16 LEAD

Ordering Information

Device	Package[2]
SC412AMLTRT[1]	MLPQ-16 3X3
SC412AEVB	Evaluation Board

Notes:
1) Available in tape and reel packaging only. A reel contains 3000 devices.
2) Available in lead-free packaging only. This product is fully WEEE, RoHS and J-TD-020B compliant. This component and all homogenous sub-components are RoHS compliant.

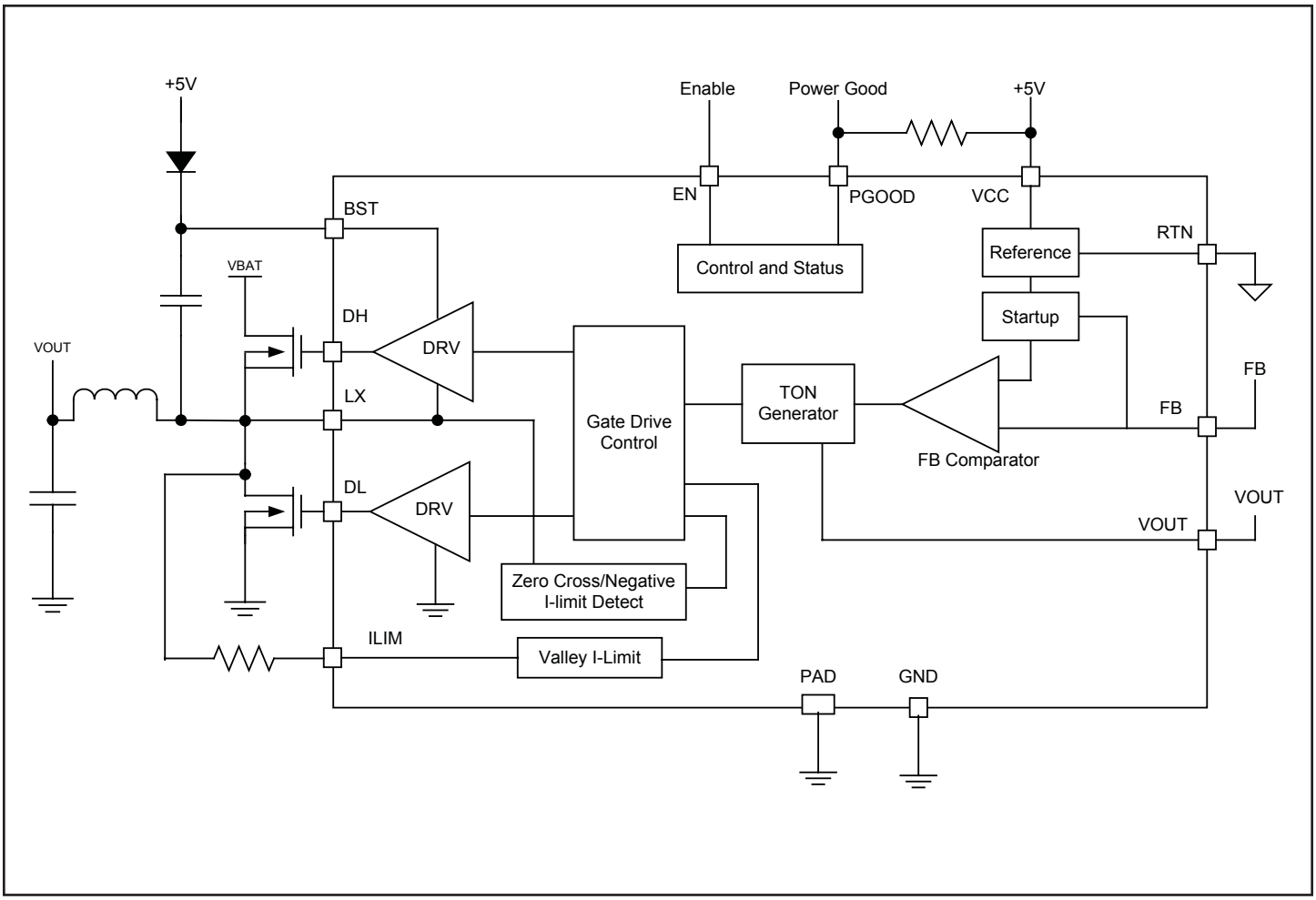
Marking Information

Marking for the 3 x 3mm MLPQ 16 Lead Package
nnnn = Part Number (example: 412A)
yyww = Date Code (example: 0652)
xxxx = Semtech Lot No. (example: E901)

Pin Descriptions

Pin #	Pin Name	Pin Function
1	LX	Switching (phase) node
2	BST	Boost capacitor connection for high-side gate drive
3	VCC	5V power input for internal analog circuits and gate drive outputs
4	DL	Gate drive output for the low-side external MOSFET
5	GND	Power ground — the return point for the DL driver output and the reference point for the ILIM and Zero Cross circuits
6	RTN	Return or analog ground for VOUT sense — connect to GND at the chip
7	NC	Not connected internally — leave unconnected or connect to GND
8	NC	Not connected internally — leave unconnected or connect to GND
9	FB	Feedback input — connect to an external resistor divider from VOUT to program the output voltage
10	VOUT	Output voltage sense point for determining the on-time
11	PGOOD	Open-drain Power Good indicator — high impedance indicates power is good — an external pull-up resistor is required.
12	EN	Enable input — connect EN to RTN to disable the SC412A
13	ILIM	Current limit sense point — to program the current limit connect a resistor from ILIM to LX or to a current sense resistor
14	NC	Not connected internally — leave unconnected or connect to GND
15	NC	Not connected internally — leave unconnected or connect to GND
16	DH	Gate drive output for the high-side external FET
T	PAD	Thermal pad for heatsinking purposes — not connected internally — connect to system ground through preferably one large via or multiple smaller vias

Block Diagram



Block Diagram

Applications Information

SC412A Synchronous Buck Controller

The SC412A is a synchronous power supply controller which simplifies the task of designing a power supply suitable for powering low voltage circuits.

Battery and +5V Bias Supplies

The SC412A requires an external +5V bias supply in addition to the battery. If stand-alone capability is required, the +5V supply can be generated with an external linear regulator.

Pseudo-Fixed-Frequency Constant On-Time PWM Controller

The PWM control method is a constant-on-time, pseudo-fixed-frequency PWM controller, see Figure 1. The ripple voltage seen across the output capacitor's ESR provides the PWM ramp signal, eliminating the need for a current sense resistor. The on-time is determined by an internal one-shot whose period is proportional to output voltage, and inversely proportional to input voltage. A separate one-shot sets the minimum off-time (typically 350ns).

The typical operating frequency is 325kHz. It is possible to raise or lower the operating frequency with external components, refer to the section on Switching Frequency Variations.

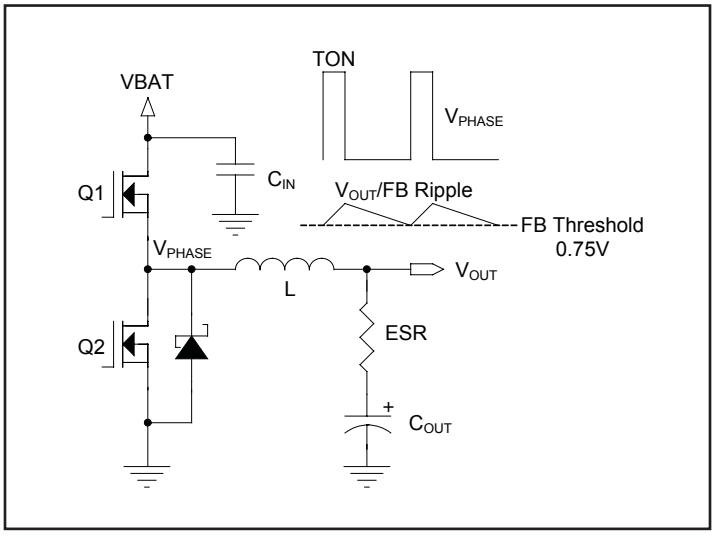


Figure 1.

On-Time One-Shot (T_{ON})

The internal on-time one-shot comparator has two inputs. One input looks at the output voltage via the VOUT pin, while the other input samples the input voltage via the LX pin and converts it to a proportional current which charges an internal on-time capacitor.

The TON time is the time required for this capacitor to charge from zero volts to VOUT, thereby making the on-time directly proportional to output voltage and inversely proportional to input voltage. This implementation results in a fairly constant switching frequency without the need of a clock generator. The internal frequency is optimized for 325kHz. The general equation for the on-time is:

$$T_{ON}\ (nsec) = 2560 \bullet (V_{OUT}/V_{BAT}) + 35$$

VOUT Voltage Selection

Output voltage is regulated by comparing VOUT as seen through a resistor divider to the internal 0.75V reference, see Figure 2. The output voltage is set by the equation:

$$V_{OUT} = 0.75 \bullet (1 + R1/R2)$$

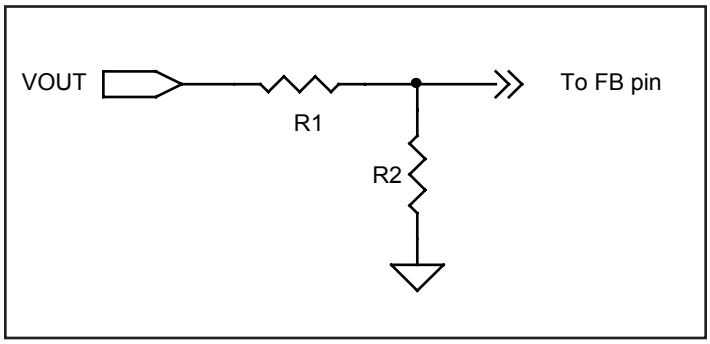


Figure 2.

Applications Information *(continued)*

Enable Input

The EN is used to disable or enable the SC412A. When EN is low (grounded), the SC412A is off and in its lowest-power state. When EN is high the controller is enabled and switching will begin.

PSAVE Operation

The SC412A provides automatic power save operation at light loads. The internal Zero-Cross comparator looks for inductor current (via the voltage across the lower MOSFET) to fall to zero on 8 consecutive cycles. Once observed, the controller then enters power save and turns off the low-side MOSFET on each cycle when the current crosses zero. To add hysteresis, the on-time is increased by 25% in power-save. The efficiency improvement at light loads more than offsets the disadvantage of slightly higher output ripple. If the inductor current does not cross zero on any switching cycle, the controller immediately exits power save. Since the controller counts zero crossings, the converter can sink current as long as the current does not cross zero on eight consecutive cycles. This allows the output voltage to recover quickly in response to negative load steps.

Smart Power Save Protection

In some applications, active loads can leak current from a higher voltage and thereby cause VOUT to slowly rise and reach the OVP threshold, leading to a hard shutdown. The SC412A uses Smart Power Save to prevent this. When the feedback signal exceeds 8% above nominal (810mV), the IC exits power save operation (if already active) and DL drives high to turn on the low-side MOSFET, which draws current from VOUT via the inductor. When FB drops back to the 0.75V trip point, a normal TON switching cycle begins. This method cycles energy from VOUT back to VBAT and prevents a hard OVP shutdown, and also minimizes operating power by avoiding continuous conduction-mode operation.

Current Limit Circuit

Current limiting can be accomplished in two ways. The RDSON of the lower MOSFET can be used as a current sensing element, or a sense resistor at the lower MOSFET source can be used if greater accuracy is needed. RDSON sensing is more efficient and less expensive. In both cases, the R_{ILIM} resistor sets the over-current threshold. The R_{ILIM} connects from the ILIM pin to either the lower MOSFET drain (for RDSON sensing) or the high side of the current-sense resistor. R_{ILIM} connects to a 10µA current source from the ILIM pin which turns on when the low-side MOSFET turns on, after the on-time DH pulse has completed. If the voltage drop across the sense resistor or low-side MOSFET exceeds the voltage across the R_{ILIM} resistor, current limit will activate. The high-side MOSFET will then not turn on until the voltage drop across the sense element (resistor or MOSFET) falls below the voltage across the R_{ILIM} resistor.

This current sensing scheme actually regulates the inductor valley current, see Figure 3. This means that if the current limit is set to 10A, the peak current through the inductor would be 10A plus the peak ripple current, and the average current through the inductor would be 10A plus 1/2 the peak-to-peak ripple current.

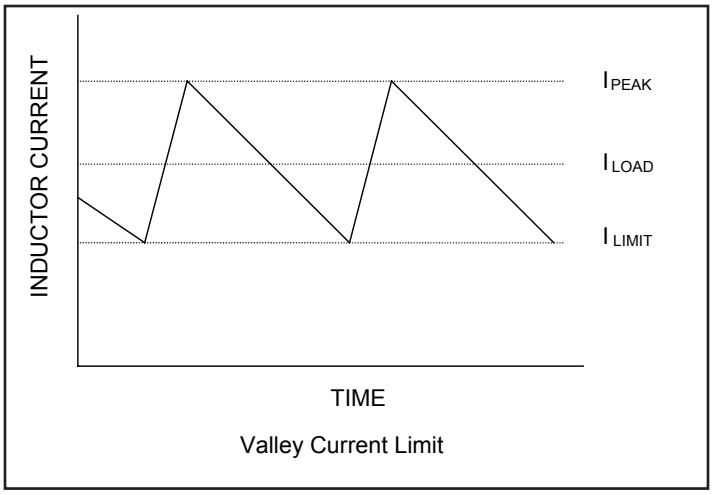


Figure 3.

Applications Information *(continued)*

The RDS_{ON} sensing circuit is shown in Figure 4 with R_{ILIM} = R1 and RDS_{ON} of Q2.

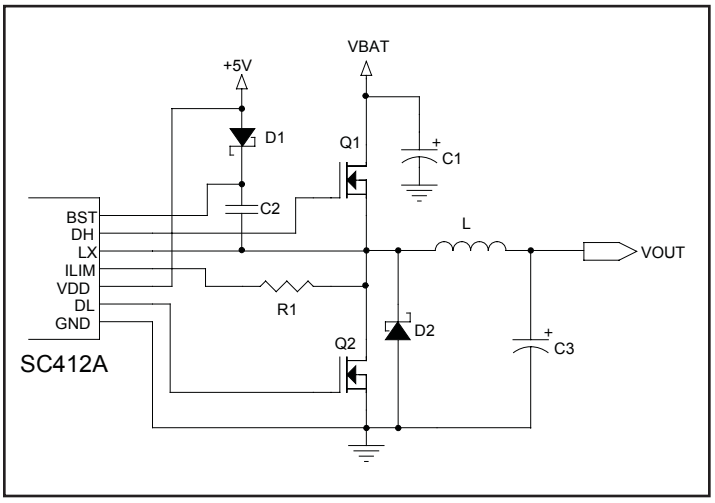


Figure 4.

The resistor sensing circuit is shown in Figure 5 with R_{ILIM} = R1 and R_{SENSE} = R4.

Resistive sensing operates similar to MOSFET sensing, except that a resistor is used to improve accuracy. The resistor connects between the MOSFET source and GND, and the RILIM connects from the ILIM pin to the sense resistor, as in Figure 5.

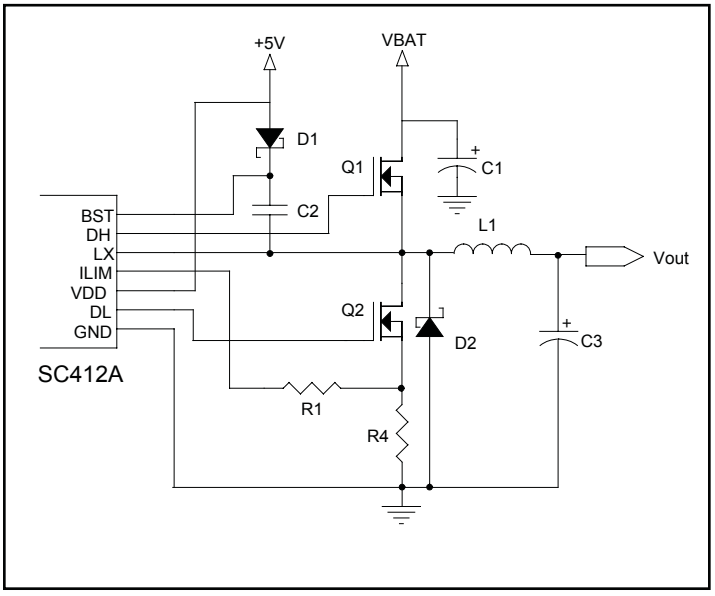


Figure 5.

The following over-current equation can be used for both RDS_{ON} or resistive sensing. For RDS_{ON} sensing, the MOSFET RDS_{ON} rating is used for the value of R_{SENSE}.

$$IL_{OC}(Valley) = 10\mu A \bullet \frac{R_{ILIM}}{R_{SENSE}}$$

Power Good Output

The power good (PGD) output is an open-drain output which requires a pull-up resistor. When the output voltage is 12% below its nominal voltage (660mV), PGD is pulled low. It is held low until the output voltage returns above approximately -11% of nominal. PGD is held low during start-up and will not be allowed to transition high until soft-start is completed (when FB reaches 0.75V). There is a 5µs delay built into the PGD circuit to prevent false transitions.

PGD also transitions low if the FB pin exceeds +20% of nominal, which is also the over-voltage shutdown point. If EN is low with VCC supplied, PGD is also pulled low.

Output Over-Voltage Protection

In steady state operation, when FB exceeds 20% of nominal, DL latches high and the low-side MOSFET is turned on. DL stays high and the SMPS stays off until the EN input is toggled or VCC is recycled. There is a 5µs delay built into the OVP detector to prevent false transitions. PGD is also low after an OVP.

Output Under-Voltage Protection

When FB falls 30% below its trip point for eight consecutive clock cycles, the output is shut off; the DL/DH drives are pulled low to tri-state the MOSFETS, and the SMPS stays off until the EN input is toggled or VCC is recycled.

POR and UVLO

Under-voltage lockout circuitry (UVLO) inhibits switching and tri-states the DH/DL drivers until VCC rises above 4.4V. An internal power-on reset (POR) occurs when VCC exceeds 4.4V, which resets the fault latch and soft-start counter, to prepare the PWM for switching. At this time the SC412A will come out of UVLO and begin the soft-start cycle.

Applications Information *(continued)*

Soft-Start

The soft-start is accomplished by ramping the FB comparator's internal reference from zero to 0.75V in 30mV increments. Each 30mV step typically lasts for eight clock cycles.

During the soft-start period, the Zero Cross Detector is active to monitor the voltage across the lower MOSFET while DL is high. If the inductor current reaches zero, the FB comparator's internal ramp reference is immediately overridden to match the voltage at the FB pin. This soon causes the FB comparator to trip which forces DL to turn off and a DH on-time will begin. This prevents the inductor current from going too negative which would cause droop in the VOUT start-up waveform. The next 30mV step on the internal reference ramp occurs from the new point at the FB pin. Since any of the internal 30mV steps can be overridden by the FB waveform, the start-up time is therefore dependent upon operating conditions. This override feature will stop when the FB pin reaches approximately 660mV.

At start-up, during the first 32 switching cycles, the overcurrent threshold is reduced by 50%, to reduce overshoot caused by the first set of switching pulses.

MOSFET Gate Drivers

The DH and DL drivers are optimized for driving moderate high-side and larger low-side power MOSFETs. An adaptive dead-time circuit monitors the DL output and prevents the high-side MOSFET from turning on until DL is fully off, and conversely, monitors the DH output and prevents the low-side MOSFET from turning on until DH is fully off. Be sure there is low resistance and low inductance between the DH and DL outputs to the gate of each MOSFET.

The SC412A utilizes SmartDrive™ to achieve fast switching with reduced noise. At the start of the DH on-time when LX is typically below GND, the DH output drives the high-side MOSFET through a pull-up resistance of 10 ohms, which results in a soft reverse-recovery of the low-side diode. The high-side MOSFET conducts and causes LX to rise; when LX reaches 1.5volts, the DH drive resistance is reduced to 2 ohms to provide fast switching and reduce switching loss.

Design Procedure

Prior to designing a switch mode supply, the input voltage, load current, switching frequency and inductor ripple current must be specified.

For notebook systems the maximum input voltage (VIN_{MAX}) is determined by the highest AC adaptor voltage, and the minimum input voltage (VIN_{MIN}) is determined by the lowest battery voltage after accounting for voltage drops due to connectors, fuses and battery selector switches.

In general, four parameters are needed to define the design:

1) Nominal output voltage (VOUT)
2) Static or DC output tolerance
3) Transient response
4) Maximum load current (IOUT)

There are two values of load current to consider: continuous load current and peak load current. Continuous load current is concerned with thermal stresses which drive the selection of input capacitors, MOSFETs and commutation diodes. Peak load current determines instantaneous component stresses and filtering requirements such as inductor saturation, output capacitors and design of the current limit circuit.

Design example:

VBAT = 10V min, 20V max
VOUT = 1.15V +/- 4%
Load = 20A maximum

Inductor Selection

Low inductor values result in smaller size, but create higher ripple current and are less efficient because of the high AC current flowing in the inductor. Higher inductor values will reduce the ripple current and are more efficient, but are larger and more costly. The inductor selection is generally based on the ripple current which is typically set between 20% to 50% of the maximum load current. Cost, size, output ripple and efficiency all play a part in the selection process.

Applications Information *(continued)*

The switching frequency is optimized for 325kHz. The equation for on-time is:

$$T_{ON}\ (nsec) = 2560 \bullet (V_{OUT}/V_{BAT}) + 35$$

During the DH on-time, voltage across the inductor is (VBAT - VOUT). To determine the inductance, the ripple current must be defined. Smaller ripple current will give smaller output ripple and but will lead to larger inductors. The ripple current will also set the boundary for PSAVE operation: the switching will typically enter PSAVE operation when the load current decreases to 1/2 of the ripple current; (i.e. if ripple current is 4A then PSAVE operation will typically start for loads less than 2A. If ripple current is set at 40% of maximum load current, then PSAVE will commence for loads less than 20% of maximum current).

The equation for determining inductance is:

$$L = (V_{BAT} - VOUT) \bullet T_{ON} / I_{RIPPLE}$$

Use the maximum value for VBAT, and for TON use the value associated with maximum VBAT.

T_{ON} = 182 nsec at 20V_{BAT}, 1.1V_{OUT}

$$L = (20 - 1.15) \bullet 182\ nsec / 5A = 0.69\mu H$$

We will select a slightly larger value of 0.7µH, which will decrease the maximum I_{RIPPLE} to 4.91A.

Note: the inductor must be rated for the maximum DC load current plus 1/2 of the ripple current.

The ripple current under minimum VBAT conditions is also checked.

$$TON_{VBATMIN} = 2560 \bullet (1.15/10) + 35 = 329\ nsec$$

$$I_{RIPPLE} = (V_{BAT} - V_{OUT}) \bullet T_{ON} / L$$

$$I_{RIPPLE\_VBATMIN} = (10 - 1.15) \bullet 329\ nsec / 0.7\mu H = 4.16A$$

Capacitor Selection

The output capacitors are chosen based on required ESR and capacitance. The ESR requirement is driven by the output ripple requirement and the DC tolerance. The output voltage has a DC value that is equal to the valley of the output ripple, plus 1/2 of the peak-to-peak ripple. Change in the ripple voltage will lead to a change in DC voltage at the output.

The design goal is +/-4% output regulation. The internal 0.75V reference tolerance is 1%, assuming 1% tolerance for the FB resistor divider, this allows 2% tolerance due to VOUT ripple. Since this 2% error comes from 1/2 of the ripple voltage, the allowable ripple is 4%, or 46mV for a 1.15V output.

The maximum ripple current of 4.05A creates a ripple voltage across the ESR. The maximum ESR value allowed would be 44mV:

$$ESR_{MAX} = V_{RIPPLE}/I_{RIPPLEMAX} = 46mV / 4.91A$$

$$ESR_{MAX} = 9.4\ m\Omega$$

The output capacitance is typically chosen based on transient requirements. A worst-case load release, from maximum load to no load at the exact moment when inductor current is at the peak, defines the required capacitance. If the load release is instantaneous (load changes from maximum to zero in a very small time), the output capacitor must absorb all the inductor's stored energy. This will cause a peak voltage on the capacitor according to the equation:

$$COUT_{MIN} = L \bullet (I_{OUT} + 1/2 \bullet I_{RIPPLEMAX})^2 / (V_{PEAK}^2 - VOUT^2)$$

Assuming a peak voltage VPEAK of 1.230 (80mV rise upon load release), and a 10 amp load release, the required capacitance is:

$$COUT_{MIN} = 0.7\mu H \bullet (10 + 1/2 \bullet 4.91)^2 / (1.23^2 - 1.15^2)$$

$$COUT_{MIN} = 570\mu F$$

Layout Guidelines

These requirements (650µF, 10.8mΩ) can be met using two capacitors, 330µF 20mΩ.

If the load release is relatively slow, the output capacitance can be reduced. At heavy loads during normal switching, when the FB pin is above the 0.75V reference, the DL output is high and the low-side mosfet is on. During this time, the voltage across the inductor is approximately - VOUT. This causes a downslope or falling di/dt in the inductor. If the load di/dt is not much faster than the di/dt in the inductor, then the inductor current can track change in load current, and there will be relatively less overshoot from a load release. The following can used to calculate the needed capacitance for a given dILOAD/dt:

Peak inductor current,

$$ILPEAK = I_{LOADMAX} + 1/2 \bullet I_{RIPPLEMAX}$$

$$ILPEAK = 10 + 1/2 \bullet 4.05 = 12.02A$$

Rate of change of Load current = dILOAD/dt

IMAX = maximum load release = 10A

$$C_{OUT} = ILPEAK \bullet \frac{(L \bullet ILPEAK / VOUT - IMAX/dILOAD/dt)}{2 \bullet (VPEAK - VOUT)}$$

Example: Load dI/dt = 2.5A/usec

This would cause the output current to move from 10A to zero in 4µsec.

$$C_{OUT} = \frac{12.45 \bullet (0.7\mu H \bullet 12.45/1.15 - 10/(2.5/1\mu sec)}{2 \bullet (1.23 - 1.15)}$$

$$C_{OUT} = 278\ \mu F$$

Stability Considerations

Unstable operation shows up in two related but distinctly different ways: double-pulsing and fast-feedback loop instability. double-pulsing occurs due to switching noise seen at the FB input or because the ESR is too low, causing insufficient voltage ramp in the FB signal. This causes the error amplifier to trigger prematurely after the 350ns minimum off-time has expired. double-pulsing will result in higher ripple voltage at the output, but in most cases is harmless. In some cases, however, double-pulsing can indicate the presence of loop instability, which is caused by insufficient ESR.

One simple way to solve this problem is to add some trace resistance in the high current output path. A side effect of doing this is output voltage droop with load. Another way to eliminate doubling-pulsing is to add a small (e.g. 10pF) capacitor across the upper feedback resistor divider network, (this capacitor is shown in Figure 6). This capacitance should be left out until confirmation that double-pulsing exists. Adding this capacitance will add a zero in the transfer function and should eliminate the problem. It is best to leave a spot on the PCB in case it is needed.

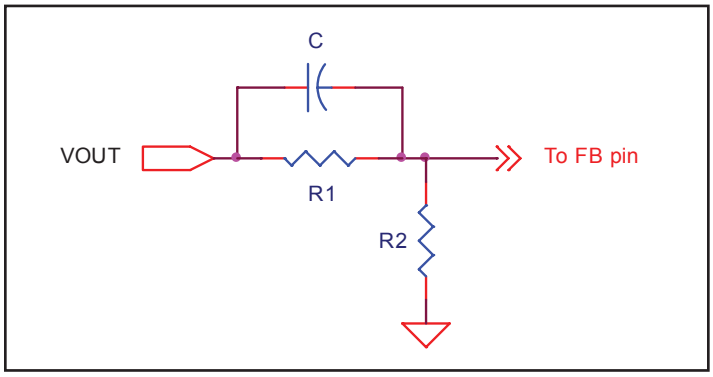


Figure 6.

Loop instability can cause oscillations at the output as a response to line or load transients. These oscillations can trip the over-voltage protection latch or cause the output voltage to fall below the tolerance limit.

The best way for checking stability is to apply a zero-to-full load transient and observe the output voltage ripple envelope for overshoot and ringing. Over one cycle of ringing after the initial step is a sign that the ESR should be increased.

Layout Guidelines *(continued)*

SC412A ESR Requirements

The constant on-time control used in the SC412A regulates the valley of the output ripple voltage. This signal consists of a term generated by the output ESR of the capacitor and a term based on the increase in voltage across the capacitor due to charging and discharging during the switching cycle. The minimum ESR is set to generate the required ripple voltage for regulation. For most applications the minimum ESR ripple voltage is dominated by PCB layout and the properties of SP or POSCAP type output capacitors. For applications using ceramic output capacitors, the absolute minimum ESR must be considered. If the ESR is low enough the ripple voltage is dominated by the charging of the output capacitor. This ripple voltage lags the on-time due to the LC poles and can cause double pulsing if the phase delay exceeds the off-time of the converter. To prevent double pulsing, the ripple voltage present at the FB pin should be 10-15mV minimum over the on-time interval.

Dropout Performance

The output voltage adjust range for continuous-conduction operation is limited by the fixed 350nS (typical) Minimum Off-time One-shot. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on and off times.

The IC duty-factor limitation is given by:

$$DUTY = \frac{T_{ON(MIN)}}{T_{ON(MIN)} + T_{OFF(MAX)}}$$

Be sure to include inductor resistance and MOSFET on-state voltage drops when performing worst-case dropout duty-factor calculations.

SC412A System DC Accuracy (VOUT Controller)

Three factors affect VOUT accuracy: the trip point of the FB error comparator, the switching frequency variation with line and load, and the external resistor tolerance. The error comparator offset is trimmed so that it trips when the feedback pin is 0.75V, 1%.

The on-time pulse in the SC412A is calculated to give a pseudo-fixed frequency of 325kHz. Nevertheless, some frequency variation with line and load is expected. This variation changes the output ripple voltage. Because constant on-time converters regulate to the valley of the output ripple, ½ of the output ripple appears as a DC regulation error. For example, If the output ripple is 50mV with VIN = 6 volts, then the measured DC output will be 25mV above the comparator trip point. If the ripple increases to 80mV with VIN = 25 volts, then the measured DC output will be 40mV above the comparator trip. The best way to minimize this effect is to minimize the output ripple.

To compensate for valley regulation it is often desirable to use passive droop. Take the feedback directly from the output side of the inductor, placing a small amount of trace resistance between the inductor and output capacitor. This trace resistance should be optimized so that at full load the output droops to near the lower regulation limit. Passive droop minimizes the required output capacitance because the voltage excursions due to load steps are reduced.

The use of 1% feedback resistors contributes up to 1% error. If tighter DC accuracy is required use 0.1% resistors.

The output inductor value may change with current. This will change the output ripple and thus the DC output voltage. The output ESR also affects the ripple and thus the DC output voltage.

Switching Frequency Variations

The switching frequency will vary somewhat due to line and load conditions. The line variations are a result of a fixed offset in the on-time one-shot, as well as unavoidable delays in the external MOSFET switching. As VBAT increases, these factors make the actual DH on-time slightly longer than the idealized on-time. The net effect is that frequency tends to falls slightly as with increasing input voltage.

The load variations are due to losses in the power train due to IR drop and switching losses. For a conventional PWM constant-frequency topology, as load increases the duty cycle also increases slightly to compensate for IR and switching losses in the MOSFETs and inductor. A constant on-time topology must also overcome the same losses

Applications Information *(continued)*

by increasing the duty cycle (more time is spent drawing energy from VBAT as losses increase). Since the on-time is constant for a given VOUT/VBAT combination, the way to increase duty cycle is to gradually shorten the off-time. The net effect is that switching frequency increases slightly with increasing load.

The typical operating frequency is 325kHz. It is possible to raise the frequency by placing a resistor divider between the output and the VOUT pin, see Figure 7. This reduces the voltage at the VOUT pin which is used to generate the on-time according to the previous equation. Note that this places a small minimum load on the output. The new frequency is approximated by the following equation:

$$FREQ\ (kHz) = 325 \cdot (1 + R1/R2)$$

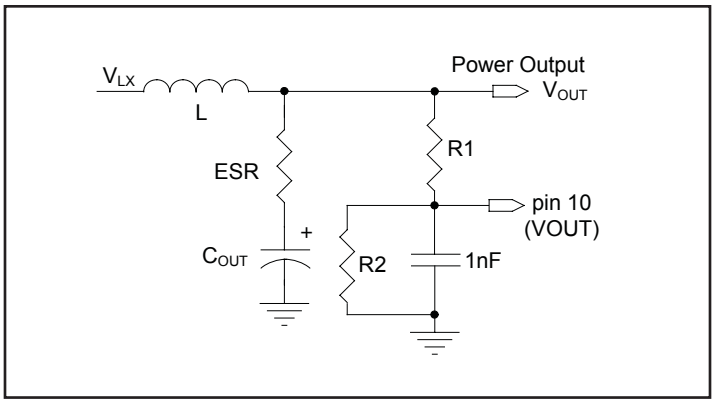


Figure 7.

It is also possible to lower the frequency using a resistive divider to the 5V bias supply, see Figure 3. This raises the voltage at the VOUT pin which will increase the on-time. Note that this results in a small leakage path from the 5V supply to the output voltage. The resistor values should be fairly large (>50kOhm) large to prevent the output voltage from drifting up during shutdown conditions. Note that the feedback resistors act as a dummy load to limit how far the output can rise.

The new operating frequency is approximated by the equation:

$$FREQ\ (kHz) = 325 \cdot ((R1 + R2) / (R1 + R2 \cdot VCC/VOUT))$$

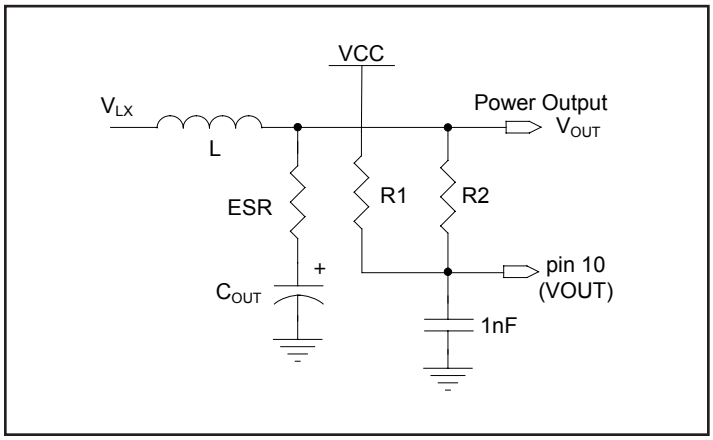


Figure 8.

Layout Guidelines

Layout Guidelines

One or more ground planes are recommended to minimize the effect of switching noise and copper losses and to maximize heat removal. The analog ground reference, RTN, should connect directly to the thermal pad, which in turn connects to the ground plane through preferably one large via. There should be a RTN plane or copper are near the chip; all components that are referenced to RTN should connect to this plane directly, not through the ground plane, and located on the chip side of the PCB if possible.

GND should be a separate plane which is not used for routing analog traces. The VCC input provides power to the internal analog circuits and the upper and lower gate drivers.

The VCC supply decoupling capacitor should be tied between VCC and GND with short traces. All power GND connections should connect directly to this plane with special attention given to avoiding indirect connections between RTN and GND which will create ground loops. As mentioned above, the RTN plane must be connected to the GND plane at the chip near the RTN/GND pins.

The switcher power section should connect directly to the ground plane(s) using multiple vias as required for current handling (including the chip power ground connections). Power components should be placed to minimize loops and reduce losses. Make all the power connections on one side of the PCB using wide copper filled areas if possible. Do not use “minimum” land patterns for power components. Minimize trace lengths and maximize trace widths between the gate drivers and the gates of the MOSFETs to reduce parasitic impedances (and MOSFET switching losses); the low-side MOSFET is most critical. Maintain a length to width ratio of <20:1 for gate drive signals. Use multiple vias as required by current handling requirement (and to reduce parasitic) if routed on more than one layer.

For an accurate ILIM current sense connection, connect the ILIM trace to the current sense element (MOSFET or resistor) directly at the pin of the element, and route that trace over to the ILIM resistor on another layer if needed. The layout can be generally considered in two parts; the control section referenced to RTN, and the switcher power section referenced to GND.

Looking at the control section first, locate all components referenced to RTN on the schematic and place these components near the chip and on the same side if possible. Connect RTN using a wide trace. Very little current flows in the RTN path and therefore large areas of copper are not needed. Connect the RTN pin directly to the thermal pad under the device as the only connection between RTN and GND.

The chip supply decoupling capacitor (VCC/GND) should be located near to the pins. Since the DL pin is directly between VCC and GND, and the DL trace must be a wide, direct trace, the VCC decoupling capacitor is best placed on the opposite side of the PCB, routed with traces as short as possible and using at least two vias when connecting through the PCB.

There are two sensitive, feedback-related pins at the chip: VOUT and FB. Proper routing is needed to keep noise away from these signals. All components connected to FB should be located directly at the chip, and the copper area of the FB node minimized. The VOUT trace that feeds into the VOUT pin, which also feeds the FB resistor divider, must be kept far away from noise sources such as switching nodes, inductors and gate drives. Route the VOUT trace in a quiet layer if possible, from the output capacitor back to the chip.

For the switcher power section, there are a few key guidelines to follow:

Layout Guidelines *(continued)*

1) There should be a very small input loop between the input capacitors, MOSFETs, inductor, and output capacitors. Locate the input decoupling capacitors directly at the MOSFETs.

2) The phase node should be a large copper pour, but still compact since this is the noisiest node.

3) The power GND connection between the input capacitors, low-side MOSFET, and output capacitors should be as small as is practical, with wide traces or planes.

4) The impedance of the power GND connection between the low-side MOSFET and the GND pin should be minimized. This connection must carry the DL drive current, which has high peaks at both rising and falling edges. Use multiple layers and multiple vias to minimize impedance, and keep the distance as short as practical.

Finally, connecting the control and switcher power sections should be accomplished as follows:

1) Route the VOUT feedback trace in a “quiet” layer, away from noise sources.

2) Route DL, DH and LX (low side FET gate drive, high side FET gate drive and phase node) to the chip using wide traces, with multiple vias if using more than one layer. These connections are to be as short as possible for loop minimization, with a length to width ratio less than 20:1 to minimize impedance. DL is the most critical gate drive, with power GND as its return path. LX is the noisiest node in the circuit, switching between VBAT and ground at high frequencies, thus should be kept as short as practical. DH has LX as its return path. DL, DH, LX, and BST are high-noise signals and should be kept well away from sensitive signals, particularly FB and VOUT.

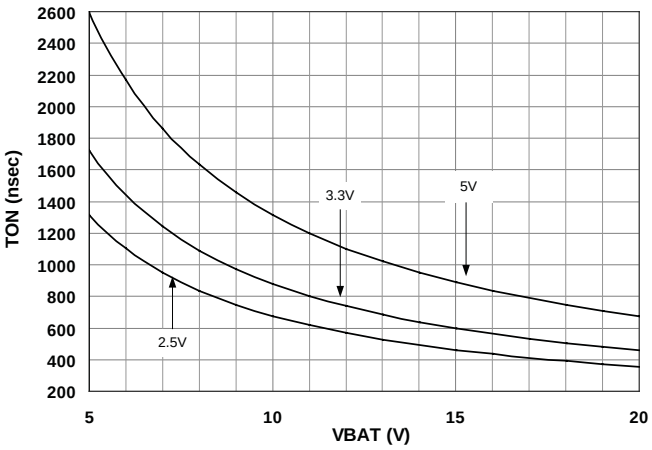
3) BST is also a noisy node and should be kept as short as possible. The high-side DH driver is relies on the boost capacitor to provide the DH drive current, so the boost capacitor must be placed near the IC and connect to the BST and LX pins using short, wide traces to minimize impedance.

4) Connect the GND pin on the chip to the VCC decoupling capacitor and then drop vias directly to the ground plane.

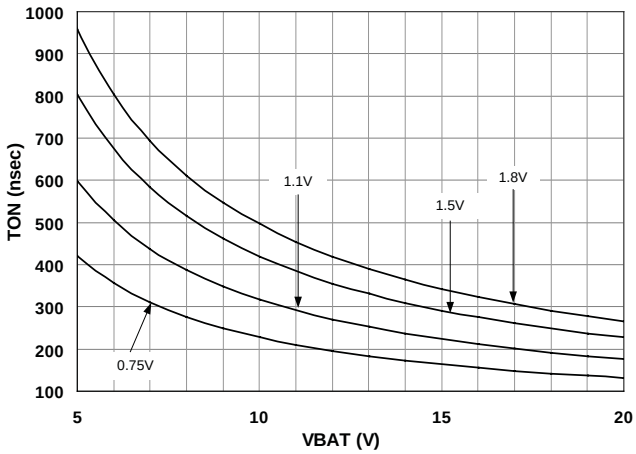
Locate the current limit resistor RLIM at the chip with a kelvin connection to the drain of the lower MOSFET at the phase node, and minimize the copper area of the ILIM trace.

Typical Characteristics

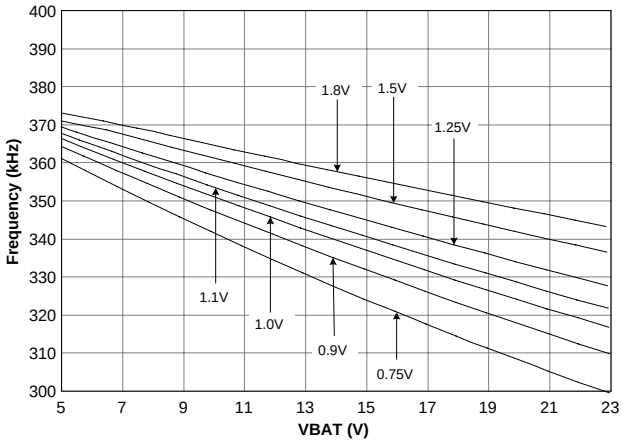
TON vs. VBAT - VOUT ≥ 2.5V



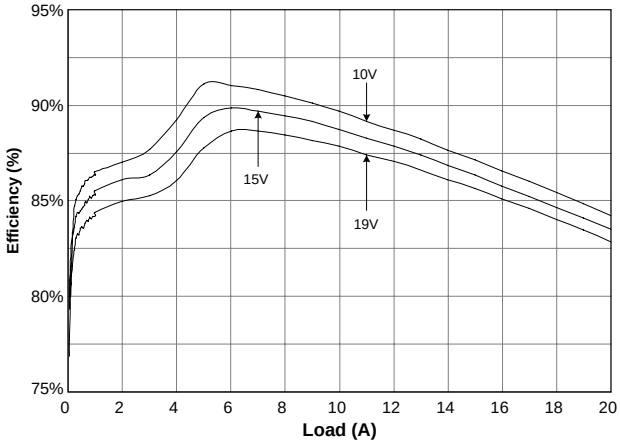
TON vs. VBAT - VOUT ≤ 1.8V



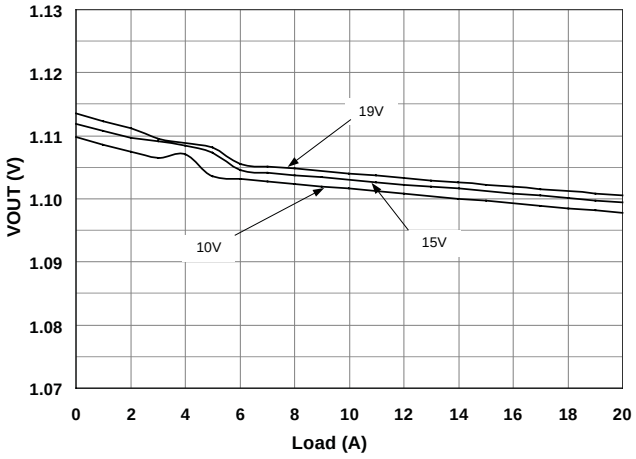
Frequency vs. VBAT



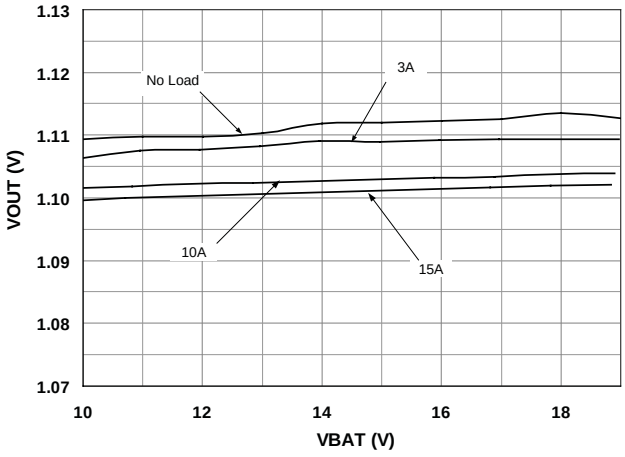
Efficiency vs. Load - 1.15V Output



Load Regulation



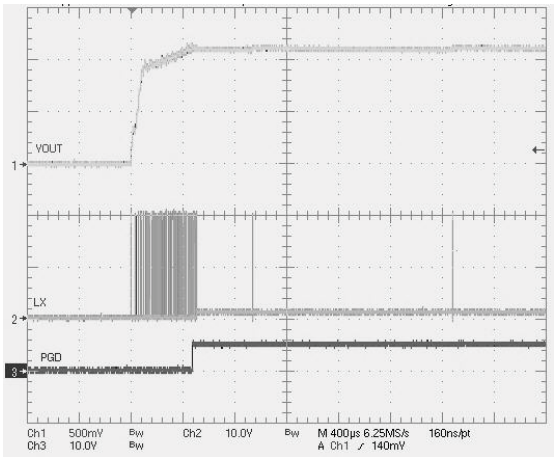
Line Regulation



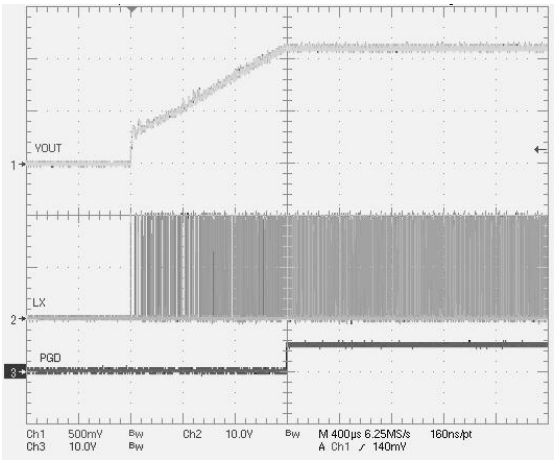
Note: See Reference schematic on Page 20.

Typical Characteristics *(continued)*

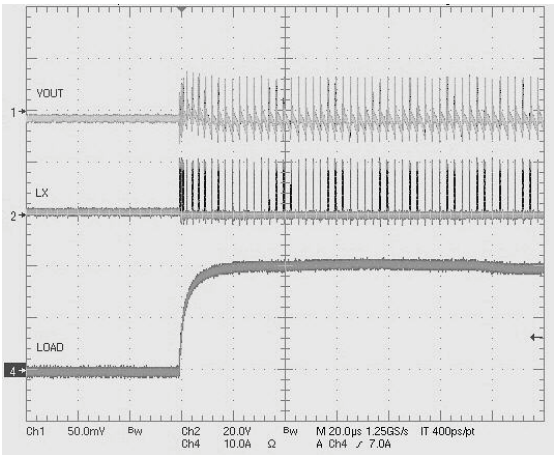
Startup 1.15V 19VBAT No load



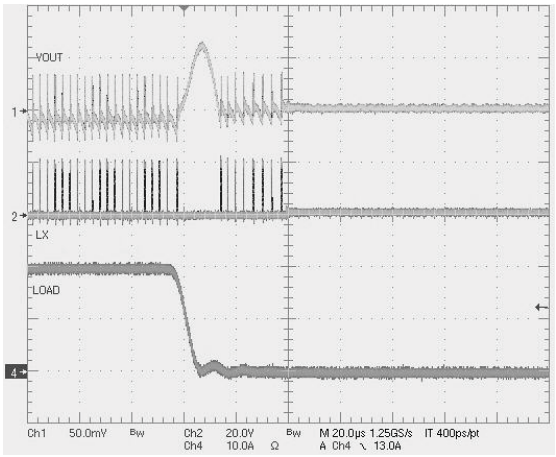
Startup 1.15V 19VBAT 20A load



Load Transient Response 0A to 20A

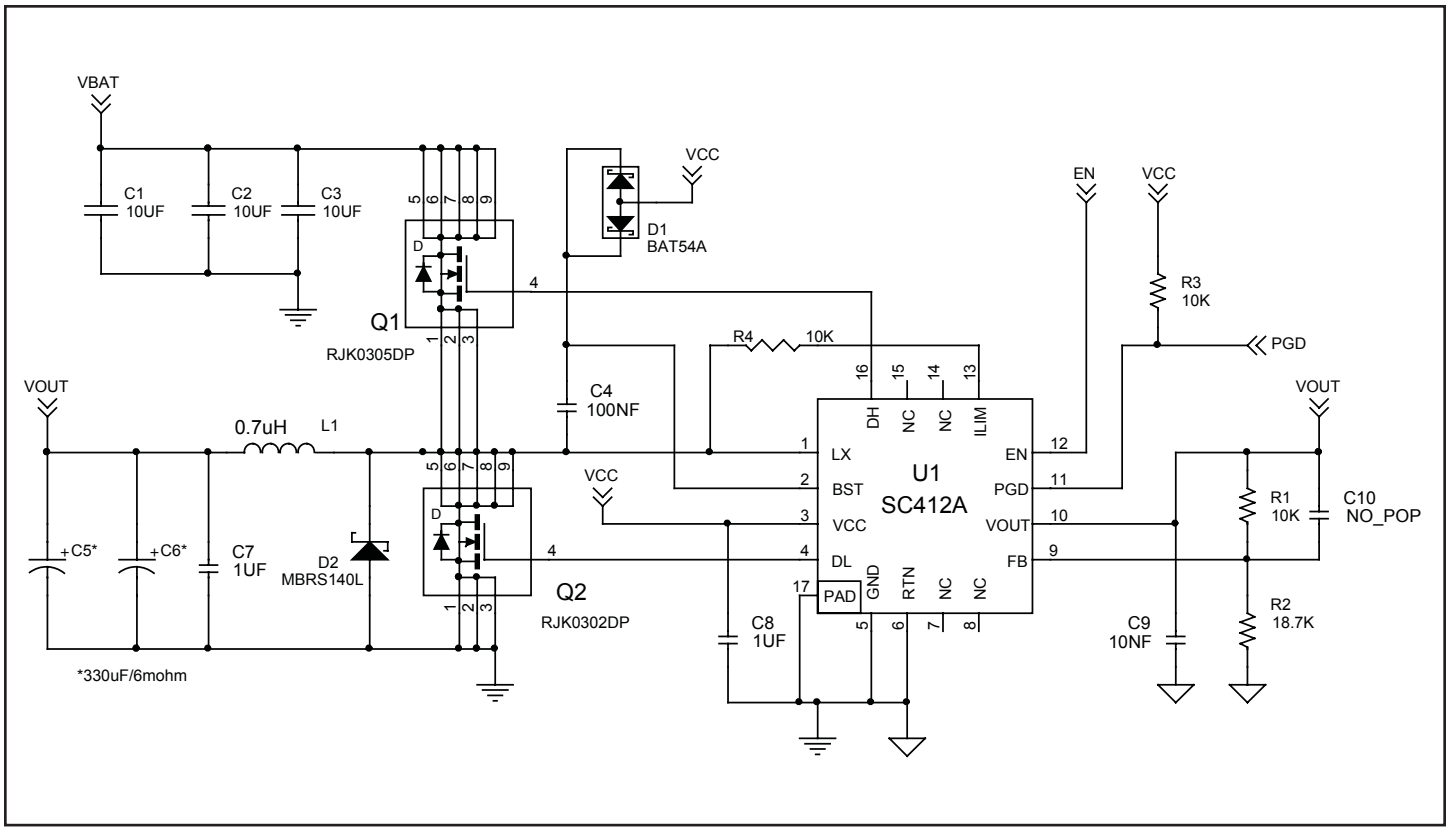


Load Transient Response 20A to 0A



Note: See Reference schematic on Page 20

Reference Design

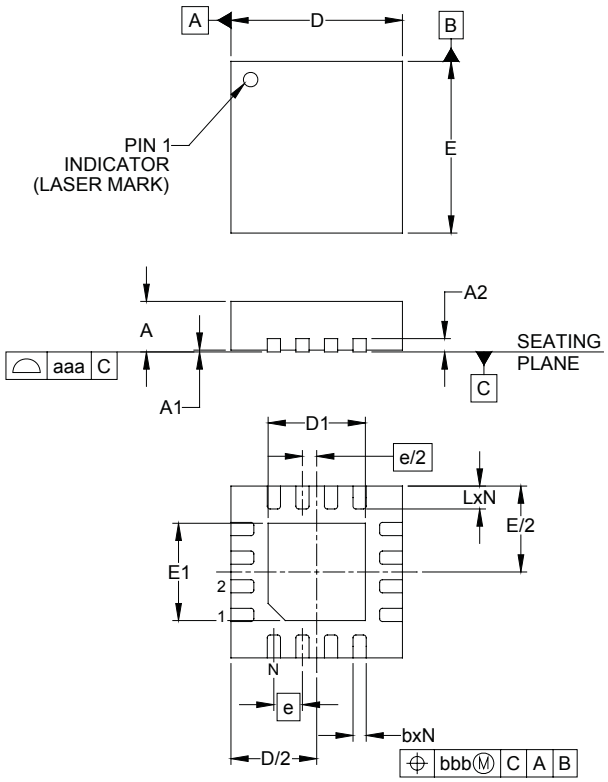


Reference Design 1.15V 20A

Bill of Materials

Component	Value	Manufacturer	Part Number	Web
C1, C2, C3	10uF, 25V	Murata	GRM32DR71E106KA12L	www.murata.com
C5, C5	330uF/6mohm/2V	Panasonic	EEFSX0D331XR	www.panasonic.com
L1	0.7uH, 24A	NEC Tokin	C-PI-1350-0R7S	http://www.nec-tokin.com
Q1	10mohm/30V	Renesas	RJK0305DBP	www.renesas.com
Q2	3.5mohm/30V	Renesas	RJK0302	www.renesas.com
D1	200mA/30V	OnSemi	BAT54C	www.onsemi.com
D2	1A/40V	OnSemi	MBSR140LT3	www.onsemi.com

Outline Drawing - MLPQ-16 3x3

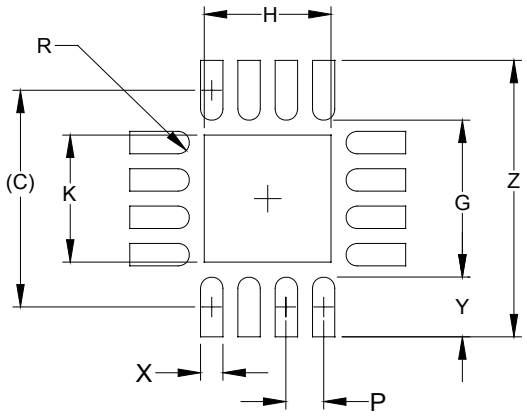


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.040	0.80	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.009	.012	0.18	0.23	0.30
D	.114	.118	.122	2.90	3.00	3.10
D1	.061	.067	.071	1.55	1.70	1.80
E	.114	.118	.122	2.90	3.00	3.10
E1	.061	.067	.071	1.55	1.70	1.80
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	16			16		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. DAP IS 1.90 x 1.90mm.

Land Pattern - MLPQ-16 3x3



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.114)	(2.90)
G	.083	2.10
H	.067	1.70
K	.067	1.70
P	.020	0.50
R	.006	0.15
X	.012	0.30
Y	.031	0.80
Z	.146	3.70

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

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