

### POWER MANAGEMENT

#### Description

The SC900 is a highly integrated power management device for low power portable applications. The device contains five adjustable low-dropout linear regulators (LDOs) with CMOS pass-devices as well as a band-gap reference, I<sup>2</sup>C interface, and DACs to control the output voltages.

Many features of the SC900 are programmable through the I<sup>2</sup>C interface. These include the ability to independently turn on any combination of the five regulators. All five of the LDO output voltages are programmable in 50mV steps from 1.45V to 3.00V. Each LDO can have an active shutdown or nonactive shutdown program option through the interface. There is also a reset monitor flag that is associated with LDOA. In addition, the device has a separate programmable power-good monitor flag that activates when one or more LDOs go out of regulation.

The SC900 offers significant quiescent current and space savings to the system designer by sharing reference and biasing among five LDOs. The small and thermally efficient 20-lead MLPQ package make it ideal for use in portable products where minimizing layout area is critical.

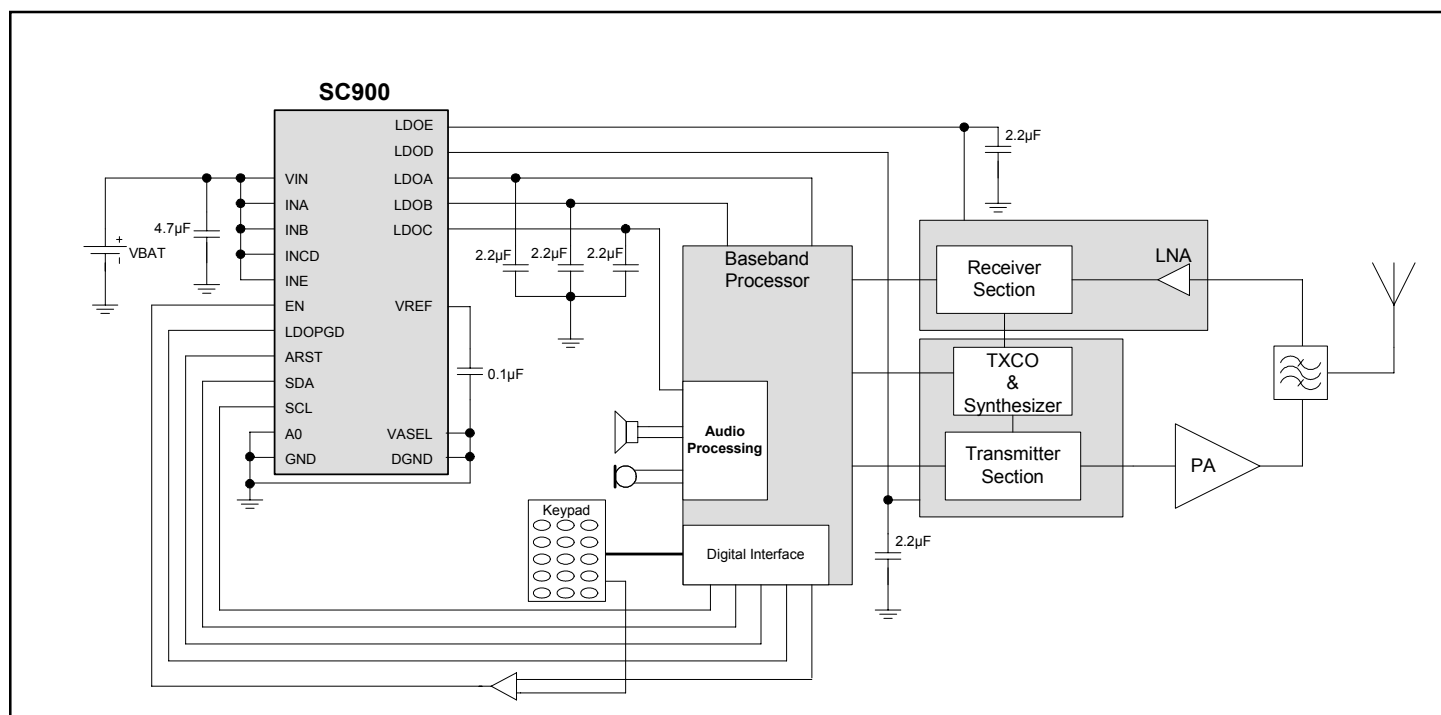
#### Features

- ◆ Five LDO regulators in one package
- ◆ I<sup>2</sup>C interface with multiple device capability
- ◆ Independent I<sup>2</sup>C enable/disable of LDOs
- ◆ Independent I<sup>2</sup>C control of output voltages
- ◆ Low thermal impedance of 40°C per watt
- ◆ 150mV dropout at 150mA
- ◆ Input range from 2.7V to 5.5V
- ◆ Programmable power-good flag
- ◆ Minimal number of external components
- ◆ Over temperature protection
- ◆ Small 4mm x 4mm 20-lead MLPQ package
- ◆ Small input/output filter capacitors
- ◆ Programmable V<sub>OUT</sub> range - 1.45V to 3.00V for each LDO

#### Applications

- ◆ Palmtop/Laptop computers
- ◆ Personal Digital Assistants
- ◆ Cellular telephones
- ◆ Battery-powered equipment
- ◆ High efficiency linear power supplies

#### Typical Application Circuit



## POWER MANAGEMENT

### Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

| Parameter                              | Symbol        | Maximum              | Units |
|----------------------------------------|---------------|----------------------|-------|
| Input Supply Voltage                   | $V_{IN}$      | -0.3 to +7           | V     |
| Digital Input Voltage                  | $V_{DIG}$     | -0.3 to $V_{IN}+0.3$ | V     |
| Operating Ambient Temperature Range    | $T_A$         | -40 to +85           | °C    |
| Operating Junction Temperature Range   | $T_J$         | -40 to +125          | °C    |
| Peak IR Reflow Temperature             | $T_{LEAD}$    | 260                  | °C    |
| Storage Temperature                    | $T_{STG}$     | -60 to +150          | °C    |
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | * 40                 | °C/W  |

\*1 Square inch, 2 ounce copper.

### Electrical Characteristics

Unless otherwise noted:  $V_{IN} = 3.7V$ ,  $EN = V_{IN}$ ,  $T_A = -40$  to  $85^{\circ}C$ . Typical values are at  $T_A = +25^{\circ}C$ .

| Parameter                              | Symbol           | Condition                                   | Min  | Typ   | Max | Units     |
|----------------------------------------|------------------|---------------------------------------------|------|-------|-----|-----------|
| <b>General</b>                         |                  |                                             |      |       |     |           |
| Supply Voltage                         | $V_{IN}$         | All outputs < $V_{IN}$ - dropout            | 2.7  |       | 5.5 | V         |
| Quiescent Current Shutdown             | $I_{Q-SHUTDOWN}$ |                                             |      |       | 10  | $\mu A$   |
| Supply Bypass Capacitor                | $C_{VCC}$        | Per input pin                               |      | 1     |     | $\mu F$   |
| <b>Digital Inputs</b>                  |                  |                                             |      |       |     |           |
| Digital Input Voltage                  | $V_{IL}$         |                                             |      |       | 0.4 | V         |
|                                        | $V_{IH}$         |                                             | 1.6  |       |     | V         |
| Digital Input Current                  | $I_{DIG}$        |                                             | -0.2 |       | 0.2 | $\mu A$   |
| <b>Digital Outputs</b>                 |                  |                                             |      |       |     |           |
| Digital Output Voltage <sup>(1)</sup>  | $V_{OL}$         | $I_{SINK} = 1.2mA$ , $V_{LDOB} \geq 1.8V$   |      | 2     | 10  | %<br>LDOB |
|                                        | $V_{OH}$         | $I_{SOURCE} = 0.5mA$ , $V_{LDOB} \geq 1.8V$ | 90   | 98    |     | %<br>LDOB |
| <b>Reference and Biasing Circuitry</b> |                  |                                             |      |       |     |           |
| Quiescent Current Reference            | $I_{Q-REF}$      |                                             |      | 25    |     | $\mu A$   |
| Reference Voltage                      | $V_{REF}$        |                                             |      | 1.227 |     | V         |
| $V_{REF}$ Start-up Time                | $t_{VREF}$       | $C_{VREF} = 100nF$                          |      | 15    |     | ms        |

**POWER MANAGEMENT**
**Electrical Characteristics (Cont.)**

Unless otherwise noted:  $V_{IN} = 3.7V$ ,  $EN = V_{IN}$ ,  $T_A = -40$  to  $85^\circ C$ . Typical values are at  $T_A = +25^\circ C$ .

| Parameters                                     | Symbol      | Conditions                                                                                                                 | Min  | Typ              | Max       | Units         |
|------------------------------------------------|-------------|----------------------------------------------------------------------------------------------------------------------------|------|------------------|-----------|---------------|
| <b>Reference and Biasing Circuitry (cont.)</b> |             |                                                                                                                            |      |                  |           |               |
| VREF Bypass Capacitor                          | CVREF       |                                                                                                                            |      | 0.1              |           | $\mu F$       |
| <b>LDO Regulators</b>                          |             |                                                                                                                            |      |                  |           |               |
| Quiescent Supply Current                       | $I_Q$       | All LDOs active in default states                                                                                          |      | 190              | 360       | $\mu A$       |
| Quiescent Supply Current at Start-up           | $I_{QSUP}$  | LDO A, B, C active in default states<br>$V_{OUT} + 0.5V < V_{IN} < 5.5V$                                                   |      | 125              |           | $\mu A$       |
| Dropout Voltage<br>LDO B,C,D,E                 | $V_D$       | $V_{OUT} = 3.0V$ , $I_{OUT} = 1mA$<br>$V_{OUT} = 3.0V$ , $I_{OUT} = 50mA$<br>$V_{OUT} = 3.0V$ , $I_{OUT} = 150mA$          |      | 1.1<br>50<br>150 | 64<br>190 | mV            |
| LDO A                                          |             | $V_{OUT} = 3.0V$ , $I_{OUT} = 200mA$                                                                                       |      | 200              | 250       |               |
| Current Limit                                  | $I_{LIM}$   |                                                                                                                            | 250  | 410              | 650       | mA            |
| Power Supply Rejection Ratio                   | PSRR        | $f = 10Hz - 1kHz$ , $C_{BYP} = 0.1\mu F$ ,<br>$I_{OUT} = 50mA$<br>$2.5V < V_{OUT} < 3.0V$                                  |      | 60               |           | dB            |
| Output Voltage Noise <sup>(2)</sup>            | $e_n$       | $f = 10Hz$ to $100kHz$ , $I_{OUT} = 50mA$<br>$C_{VREF} = 0.1\mu F$ , $C_{OUT} = 2.2\mu F$<br>$2.5V \leq V_{OUT} \leq 3.0V$ |      | 45               |           | $\mu V_{rms}$ |
| Bypass Capacitor                               | $C_{BYP}$   | Ceramic, low ESR                                                                                                           | 2.2  |                  |           | $\mu F$       |
| <b>LDO Regulator A (CORE SUPPLY)</b>           |             |                                                                                                                            |      |                  |           |               |
| Output Voltage Accuracy                        | $VOA_A$     | $1.45V \leq V_{OUT} \leq 3.00V$<br>$V_{OUT} + 0.2V \leq V_{IN} \leq 5.5V$<br>$I_{OUT} = 1mA$ , $T_A = 25^\circ C$          | -3   |                  | +3        | %             |
| Output Voltage Accuracy at 2.80V (DAC=11011)   | $VOAS_A$    | $I_{OUT} = 1mA$                                                                                                            | -2   |                  | +2        | %             |
| Output Voltage Accuracy at 1.80V (DAC=00111)   |             | $I_{OUT} = 1mA$ , $T_A = 25^\circ C$                                                                                       | -3   |                  | +3        | %             |
| Output Voltage Accuracy at 2.80V (DAC=11011)   |             | $I_{OUT} = 200mA$ , $V_{OUT} + 0.5V \leq V_{IN} \leq 5.5V$                                                                 | -3.5 |                  | +3.5      | %             |
| Maximum Output Current                         | $IOMAX_A$   |                                                                                                                            | 200  |                  |           | mA            |
| Default Setting: ON                            | $VO_{A-HI}$ | VASEL – High                                                                                                               |      | 2.80             |           | V             |
|                                                | $VO_{A-LO}$ | VASEL – Low                                                                                                                |      | 1.80             |           | V             |
| Line Regulation at 1.8V, 2.8V                  | $LINEREG_A$ | $I_{OUT} = 1mA$ , $V_{OUT} + 0.2V < V_{IN} < 5.5V$                                                                         |      | 2.5              | 12        | mV            |
| Load Regulation at 1.8V, 2.8V                  | $LOADREG_A$ | $1mA < I_{OUT} < 200mA$                                                                                                    |      | -3               | -20       | mV            |

**POWER MANAGEMENT**
**Electrical Characteristics (Cont.)**

Unless otherwise noted:  $V_{IN} = 3.7V$ ,  $EN = V_{IN}$ ,  $T_A = -40$  to  $85^\circ C$ . Typical values are at  $T_A = +25^\circ C$ .

| Parameter                                    | Symbol      | Condition                                                                                                       | Min  | Typ  | Max  | Units |
|----------------------------------------------|-------------|-----------------------------------------------------------------------------------------------------------------|------|------|------|-------|
| <b>LDO Regulator B (DIGITAL I/O SUPPLY)</b>  |             |                                                                                                                 |      |      |      |       |
| Output Voltage Accuracy                      | $VOA_B$     | $1.45V \leq V_{OUT} \leq 3.00V$<br>$V_{OUT} + 0.15V \leq V_{IN} \leq 5.5V$<br>$I_{OUT} = 1mA, T_A = 25^\circ C$ | -3   |      | +3   | %     |
| Output Voltage Accuracy at 2.80V (DAC=11011) | $VOAS_B$    | $I_{OUT} = 1mA$                                                                                                 | -2   |      | +2   | %     |
|                                              |             | $I_{OUT} = 150mA, V_{OUT} + 0.5V \leq V_{IN} \leq 5.5V$                                                         | -3.5 |      | +3.5 | %     |
| Maximum Output Current                       | $IOMAX_B$   |                                                                                                                 | 150  |      |      | mA    |
| Default Setting: ON                          | $VO_B$      |                                                                                                                 |      | 2.80 |      | V     |
| Line Regulation 2.80V                        | $LINEREG_B$ | $I_{OUT} = 1mA, V_{OUT} + 0.15V \leq V_{IN} \leq 5.5V$                                                          |      | 2.5  | 12   | mV    |
| Load Regulation at 2.80V                     | $LOADREG_B$ | $1mA < I_{OUT} < 150mA$                                                                                         |      | -3   | -20  | mV    |
| <b>LDO Regulator C</b>                       |             |                                                                                                                 |      |      |      |       |
| Output Voltage Accuracy                      | $VOA_C$     | $1.45V \leq V_{OUT} \leq 3.00V$<br>$V_{OUT} + 0.15V \leq V_{IN} \leq 5.5V$<br>$I_{OUT} = 1mA, T_A = 25^\circ C$ | -3   |      | +3   | %     |
| Output Voltage Accuracy at 2.60V (DAC=10111) | $VOAS_C$    | $I_{OUT} = 1mA$                                                                                                 | -2   |      | +2   | %     |
|                                              |             | $I_{OUT} = 150mA, V_{OUT} + 0.5V \leq V_{IN} \leq 5.5V$                                                         | -3.5 |      | +3.5 | %     |
| Maximum Output Current                       | $IOMAX_C$   |                                                                                                                 | 150  |      |      | mA    |
| Default Setting: ON                          | $VO_C$      |                                                                                                                 |      | 2.60 |      | V     |
| Line Regulation at 2.60V                     | $LINEREG_C$ | $I_{OUT} = 1mA, V_{OUT} + 0.15V < V_{IN} < 5.5V$                                                                |      | 2.5  | 12   | mV    |
| Load Regulation at 2.60V                     | $LOADREG_C$ | $1mA < I_{OUT} < 150mA$                                                                                         |      | -3   | -20  | mV    |
| <b>LDO Regulator D</b>                       |             |                                                                                                                 |      |      |      |       |
| Output Voltage Accuracy                      | $VOA_D$     | $1.45V \leq V_{OUT} \leq 3.00V$<br>$V_{OUT} + 0.15V \leq V_{IN} \leq 5.5V$<br>$I_{OUT} = 1mA, T_A = 25^\circ C$ | -3   |      | +3   | %     |
| Output Voltage Accuracy at 2.80V (DAC=11011) | $VOAS_D$    | $I_{OUT} = 1mA$                                                                                                 | -2   |      | +2   | %     |
|                                              |             | $I_{OUT} = 150mA, V_{OUT} + 0.5V \leq V_{IN} \leq 5.5V$                                                         | -3.5 |      | +3.5 | %     |
| Maximum Output Current                       | $IOMAX_D$   |                                                                                                                 | 150  |      |      | mA    |
| Default Setting: OFF                         | $VO_D$      |                                                                                                                 |      | 2.80 |      | V     |
| Line Regulation at 2.80V                     | $LINEREG_D$ | $I_{OUT} = 1mA, V_{OUT} + 0.15V < V_{IN} < 5.5V$                                                                |      | 2.5  | 12   | mV    |
| Load Regulation at 2.80V                     | $LOADREG_D$ | $1mA < I_{OUT} < 150mA$                                                                                         |      | -3   | -20  | mV    |

**POWER MANAGEMENT**
**Electrical Characteristics (Cont.)**

Unless otherwise noted:  $V_{IN} = 3.7V$ ,  $EN = VIN$ ,  $T_A = -40$  to  $85^\circ C$ . Typical values are at  $T_A = +25^\circ C$ .

| Parameter                                                                                                                                            | Symbol        | Condition                                                                                              | Min  | Typ  | Max  | Units   |
|------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|--------------------------------------------------------------------------------------------------------|------|------|------|---------|
| <b>LDO Regulator E</b>                                                                                                                               |               |                                                                                                        |      |      |      |         |
| Output Voltage Accuracy                                                                                                                              | $VOA_E$       | $1.45V < V_{OUT} < 3.00V$<br>$V_{OUT} + 0.15V < V_{IN} < 5.5V$<br>$I_{OUT} = 1mA$ , $T_A = 25^\circ C$ | -3   |      | +3   | %       |
| Output Voltage Accuracy at 2.80V<br>(DAC=11011)                                                                                                      | $VOAS_E$      | $I_{OUT} = 1mA$                                                                                        | -2   |      | +2   | %       |
|                                                                                                                                                      |               | $I_{OUT} = 150mA$ , $V_{OUT} + 0.5V < V_{IN} < 5.5V$                                                   | -3.5 |      | +3.5 | %       |
| Maximum Output Current                                                                                                                               | $IOMAX_E$     |                                                                                                        | 150  |      |      | mA      |
| Default Setting: OFF                                                                                                                                 | $VO_E$        |                                                                                                        |      | 2.80 |      | V       |
| Line Regulation at 2.80V                                                                                                                             | $LINEREG_E$   | $I_{OUT} = 1mA$ , $V_{OUT} + 0.15V < V_{IN} < 5.5V$                                                    |      | 2.5  | 12   | mV      |
| Load Regulation at 2.80V                                                                                                                             | $LOADREG_E$   | $1mA < I_{OUT} < 150mA$                                                                                |      | -3   | -20  | mV      |
| <b>I<sup>2</sup>C Interface</b>                                                                                                                      |               |                                                                                                        |      |      |      |         |
| Interface complies with slave mode I <sup>2</sup> C interface as described by Philips I <sup>2</sup> C specification version 2.1 dated January 2000. |               |                                                                                                        |      |      |      |         |
| Digital Input Voltage                                                                                                                                | $V_{IL}$      |                                                                                                        |      |      | 0.4  | V       |
|                                                                                                                                                      | $V_{IH}$      |                                                                                                        | 1.6  |      |      | V       |
| SDA Output Low Level                                                                                                                                 |               | $I_{DIN}(SDA) = 3mA$                                                                                   |      |      | 0.4  | V       |
|                                                                                                                                                      |               | $I_{DIN}(SDA) = 6mA$                                                                                   |      |      | 0.6  | V       |
| Digital Input Current                                                                                                                                | $I_{DG}$      |                                                                                                        | -0.2 |      | 0.2  | $\mu A$ |
| I/O Pin Capacitance                                                                                                                                  | $C_{IN}$      |                                                                                                        |      | 10   |      | pF      |
| <b>I<sup>2</sup>C Timing</b>                                                                                                                         |               |                                                                                                        |      |      |      |         |
| Clock Frequency                                                                                                                                      | SCL           |                                                                                                        |      |      | 400  | kHz     |
| SCL Low Period                                                                                                                                       | $t_{LOW}$     |                                                                                                        | 1.3  |      |      | $\mu s$ |
| SCL High Period                                                                                                                                      | $t_{HIGH}$    |                                                                                                        | 0.6  |      |      | $\mu s$ |
| Data Hold Time                                                                                                                                       | $t_{HD\_DAT}$ |                                                                                                        | 0    |      |      | $\mu s$ |
| Data Setup Time                                                                                                                                      | $t_{SU\_DAT}$ |                                                                                                        | 100  |      |      | ns      |
| Setup Time for Repeated Start Condition                                                                                                              | $t_{SU\_STA}$ |                                                                                                        | 0.6  |      |      | $\mu s$ |
| Hold Time for Repeated Start Condition                                                                                                               | $t_{HD\_STA}$ |                                                                                                        | 0.6  |      |      | $\mu s$ |
| Setup Time for Stop Condition                                                                                                                        | $t_{SU\_STO}$ |                                                                                                        | 0.6  |      |      | $\mu s$ |
| Bus-Free Time Between STOP and START                                                                                                                 | $t_{BUF}$     |                                                                                                        | 1.3  |      |      | $\mu s$ |

## POWER MANAGEMENT

### Electrical Characteristics (Cont.)

Unless otherwise noted:  $V_{IN} = 3.7V$ ,  $EN = V_{IN}$ ,  $T_A = -40$  to  $85^{\circ}C$ . Typical values are at  $T_A = +25^{\circ}C$ .

| Parameter                  | Symbol         | Condition              | Min | Typ | Max | Units |
|----------------------------|----------------|------------------------|-----|-----|-----|-------|
| <b>A RESET</b>             |                |                        |     |     |     |       |
| Reset Threshold            | $RESET_{THLD}$ |                        |     | 77  |     | %     |
| Reset Active Timeout Delay | $t_{RD}$       | Delay in default state | 75  | 100 | 125 | ms    |
| <b>LDO POWER GOOD</b>      |                |                        |     |     |     |       |
| PGOOD Threshold            | $PGOOD_{THLD}$ |                        |     | 77  |     | %     |
| PGOOD Active Timeout Delay | $t_{PG}$       | Delay in default state | 75  | 100 | 125 | ms    |

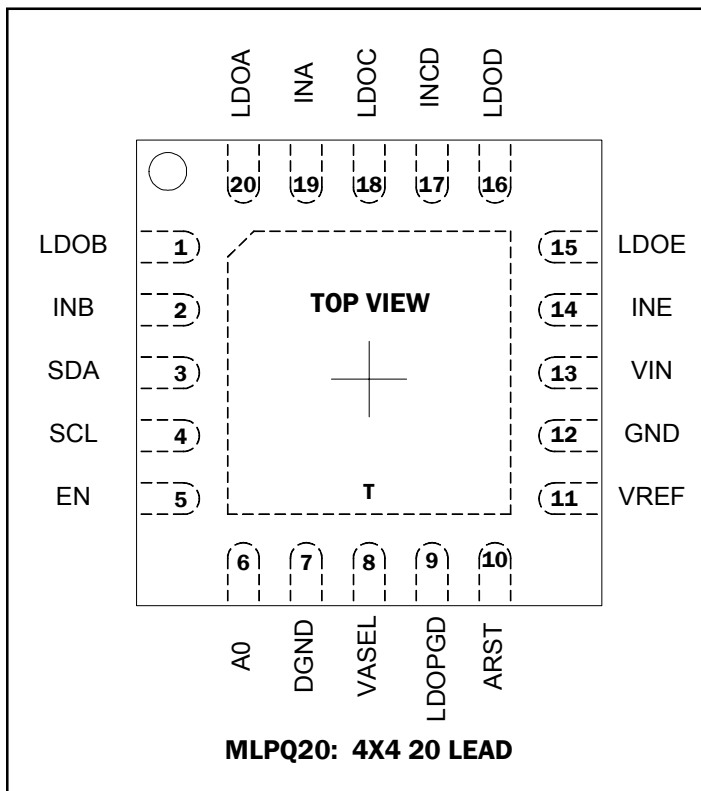
**Notes:**

(1) Digital outputs are powered from LDOB, so LDOB must be active for operation of LDOPGD and ARST.

(2) Below 2.5V: becomes digital regulator.

## POWER MANAGEMENT

### Pin Configuration



### Ordering Information

| DEVICE                     | PACKAGE <sup>(1)</sup> |
|----------------------------|------------------------|
| SC900IMLTRT <sup>(2)</sup> | MLPQ20L                |
| SC900EVb                   | Evaluation Board       |

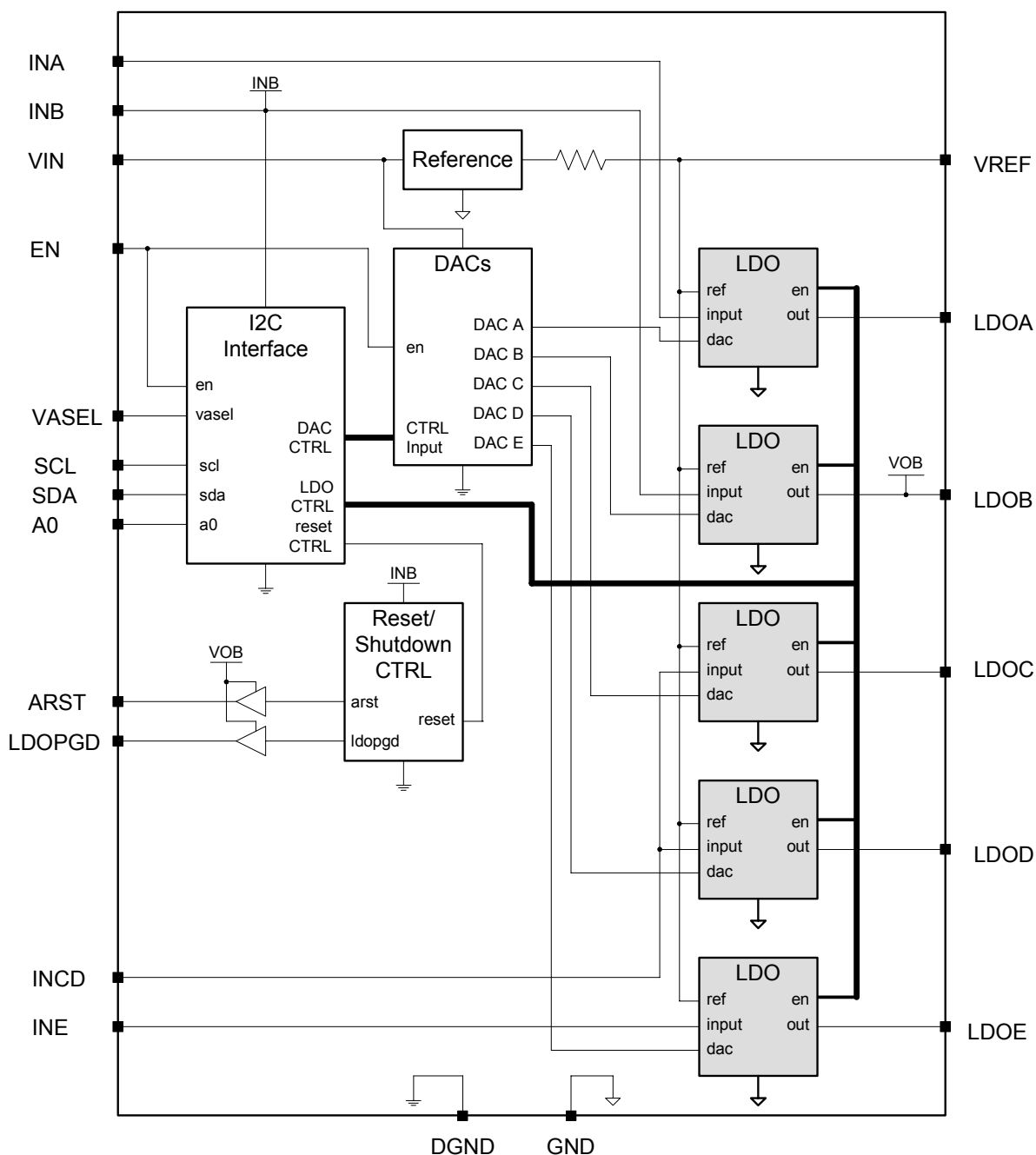
Notes:

(1) Available in tape and reel only. A reel contains 3,000 devices.

(2) Available in Lead-free package only. This product is fully WEEE and RoHS compliant.

**POWER MANAGEMENT**
**Pin Description**

| Pin# | Pin Name | Pin Function                                                                                                                                                                                |
|------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1    | LDOB     | LDO B output.                                                                                                                                                                               |
| 2    | INB      | Input supply for the digital system logic and the LDO B pass transistor.                                                                                                                    |
| 3    | SDA      | Bidirectional open drain digital I/O pin. I <sup>2</sup> C serial data.                                                                                                                     |
| 4    | SCL      | Digital input. I <sup>2</sup> C serial clock.                                                                                                                                               |
| 5    | EN       | Digital input. High to enable part. Low to disable part (sleep mode). Note I <sup>2</sup> C control is active only when part is enabled.                                                    |
| 6    | A0       | One bit address for connecting two SC900 devices onto the system through the I <sup>2</sup> C interface.                                                                                    |
| 7    | DGND     | Digital ground.                                                                                                                                                                             |
| 8    | VASEL    | LDO A selection default voltage. Tie this pin to ground for 1.8V or INB for 2.8V.                                                                                                           |
| 9    | LDOPGD   | Digital output. State change indicates that one of four LDO output voltages (A,C,D or E) is out of spec. Note, desired state of pin is programmable through the I <sup>2</sup> C interface. |
| 10   | ARST     | Digital output. State change indicates LDOA output voltage is out of spec. Note; desired state of pin is programmable through the I <sup>2</sup> C interface.                               |
| 11   | VREF     | Bandgap reference output voltage. Connect at least 0.1μF to ground ( $CV_{REF} \geq 0.1\mu F$ ).                                                                                            |
| 12   | GND      | Analog ground.                                                                                                                                                                              |
| 13   | VIN      | Analog supply voltage.                                                                                                                                                                      |
| 14   | INE      | Input supply for the LDO E pass transistor.                                                                                                                                                 |
| 15   | LDOE     | LDO E output.                                                                                                                                                                               |
| 16   | LDOD     | LDO D output.                                                                                                                                                                               |
| 17   | INCD     | Input supply for the LDO C and LDO D pass transistors.                                                                                                                                      |
| 18   | LDOC     | LDO C output.                                                                                                                                                                               |
| 19   | INA      | Input supply for the LDO A pass transistor.                                                                                                                                                 |
| 20   | LDOA     | LDO A output.                                                                                                                                                                               |
| T    | Thermal  | Pad for heat sinking purposes. Connect to ground plane using multiple vias. Not connected internally.                                                                                       |

**POWER MANAGEMENT**
**Block Diagram**


## POWER MANAGEMENT

### Applications Information

#### General Description

Each of the five low-dropout linear regulators (LDOs) can be independently enabled or disabled and their output voltages can each be set by an independent DAC. These controls can be accessed through the I<sup>2</sup>C serial port. There are five 8-bit volatile registers in the SC900; one for each LDO (registers A,B,C,D,E). In addition there is one common reset and power good control register and one on/off control register. The active shutdown circuitry can be accessed through each LDO register (refer to the section “Active Shutdown” on page 11 for more information).

At power-up, the register contents are reset to their default values and the ARST for LDO A has a default start-up delay of 100ms. At any time the part can be put into its lowest power state (shutdown) by pulling the EN pin low. Whenever the EN pin is forced low, the previous settings are lost and the part requires reprogramming to return to the desired state. When EN is pulled high, the device starts up in the default state. A detailed description of the protocol used to load the registers with data is described in the section entitled “Using the I<sup>2</sup>C Interface” on page 13.

#### VIN and Enable Pin

The VIN supply must be  $\geq 2.7V$  before the EN pin can be asserted. This means that the EN pin should not be tied to VIN so that it does not reach a logic high level before the input supply reaches 2.7V.

#### LDOA (Core Supply)

LDOA is intended to be used as the MSM core supply. It has an output current capability of 200mA and a dedicated reset signal ARST. INA is the dedicated input supply for this regulator.

#### LDOB (Digital I/O Supply)

INB supplies power for the internal I<sup>2</sup>C interface and other digital I/O functions, while LDOB supplies power for ARST and LDOPGD output ports (see block diagram). Therefore it is imperative that LDOB be operational to make use of ARST and LDOPGD. If LDOB is turned off by the on/off control register, these output ports will not function.

#### LDO RESET Control Register:

##### ARST Pin

There are two functions that can be programmed, defining the ARST pin action:

- Set the polarity of the reset signal
- Set the reset clear delay time in milliseconds

As soon as the LDOA output voltage falls below its programmed value, the ARST pin is asserted. The polarity of the ARST pin can be set to active high or active low during a reset condition, by bit 6 of the LDO Reset Control Register. Once the error condition is resolved (output rises to the programmed value), a delay is initiated before the ARST pin is cleared. The delay is programmable by bits 0-1 of the LDO Reset Control Register. The Default delay time is 100ms, and the delay can be programmed for 0, 50, 100, or 150ms.

##### LDOPGD Pin

There are three functions that can be programmed to define the LDOPGD pin action:

- Set which LDOs are to be monitored for power-good
- Set the polarity of the power-good signal
- Set the power-good delay time in milliseconds

Bits 4 and 5 of the LDO Reset Control Register select which LDO or LDOs are monitored. LDO C, D and E can be monitored independently or LDOs A, C, D, & E can be monitored collectively. The polarity of the LDOPGD pin can be set to active high or active low by bit 7 of the LDO Reset Control Register. As soon as any of the selected LDO output voltages which are monitored falls within spec, the LDO power-good (LDOPGD) pin is asserted. Once the LDO output power is stable (output rises to the programmed value), a delay is initiated before the LDOPGD pin is set. The delay is programmable by bits 2 and 3 of the LDO Reset Control Register. The default delay is 100ms, and this delay can be programmed to 0, 50, 100, or 150ms.

## POWER MANAGEMENT

### Applications Information (Cont.)

#### Active Shutdown

The shutdown control bits determine how the on-chip active shutdown switches behave. Each LDO register uses bit 5 of the LDO output voltage data byte to control the shutdown behavior. When the active shutdown bit is enabled (set to 1), the capacitance on the LDO output will be discharged by an on-chip FET after the LDO is disabled. When the active shutdown bit is disabled (set to 0), the output capacitance on the LDO output is discharged by the load. The default active shutdown state for all LDOs is on.

#### ON/OFF Control Register

Each individual LDO may be turned on or off by accessing the ON/OFF control register. LDOs are turned on by setting their respective on/off bit to 1. Likewise, they can be turned off by setting the on/off bit to 0. This allows for on/off control with a single write command. If the enable (EN) pin is high and data is written to the LDO voltage registers, the LDO outputs will go to the voltage prescribed by the Output Voltage Code bits (0-4). Data will not be lost when toggling the on/off bit from 0 to 1. However, if the EN pin is forced low, all circuitry in the device is disabled. All programmed information is lost when the enable bit is subsequently pulled high.

#### VASEL Pin

The VASEL pin sets the default voltage of LDO A, the core supply. When this pin is set to VIN, the default voltage is 2.80V. When this pin is set to GND, the default voltage is 1.80V. The voltage can be changed from its default state after start up by writing to the LDO voltage code register.

#### Device Addressing

Following a start condition, the master must output the address of the slave it is accessing. The most significant six bits of the slave are the device type identifier (ID). For the SC900 this is fixed at 000100[B]. The next significant bit addresses a particular device. A system can have up to two SC900 devices on the bus. The two addresses are defined by the state of the A0 input (see Figure 1).

| DEVICE TYPE IDENTIFIER |   |   |   |   |   | DEVICE ADDRESS                         | R/W |
|------------------------|---|---|---|---|---|----------------------------------------|-----|
| 0                      | 0 | 0 | 1 | 0 | 0 | Pin A0 to GND = 0<br>Pin A0 to VIN = 1 | X   |

**Figure 1 - Slave Address Structure**

When the A0 pin is tied to GND, device 1 has an address of 0 and the combination of device type ID and address is 0x08H. When the A0 pin is tied to VIN, device 2 has an address of 1 and the combination of device type ID and address is 0x09H.

The last bit of the slave address defines the operation to be performed. When set to a one a read operation is selected; when set to a zero a write operation is selected. Following a start condition, the SC900 monitors the SDA line comparing the slave address being transmitted with its slave address (device type ID and state of A0 input). Upon a correct compare the SC900 outputs an acknowledge on the SDA line. Depending on the state of the R/W bit, the SC900 will execute a read or write operation.

#### Protection Circuitry

The SC900 provides protection circuitry that prevents the device from operating in an unspecified state. These include Under-voltage Lockout Protection, Over-temperature Protection and Short-circuit Protection.

#### Under Voltage Lockout

The SC900 provides an Under Voltage Lockout (UVLO) circuit to protect the device from operating in an unknown state if the input voltage supply is too low. When the battery voltage drops below the UVLO threshold, the LDOs are disabled. As the battery voltage increases above the hysteresis level, the LDOs are re-enabled into their previous states, provided ENABLE has remained high. If ENABLE goes low, the SC900 will shut down.

#### Over-temperature Protection

The SC900 provides an internal Over-temperature (OT) protection circuit that monitors the internal junction temperature. When the temperature exceeds the OT threshold, the OT protection disables all the LDO outputs. As the junction temperature drops below the hysteresis level the OT protection re-enables all the LDOs in their previous states, provided ENABLE has remained high. If ENABLE goes low, the SC900 will shut down.

#### Short-circuit Protection

Each LDO output has short-circuit protection. If a short is applied to any output, the output voltage will drop and the output current will be limited to the short circuit current until the short is removed.

## POWER MANAGEMENT

### Applications Information (Cont.)

#### Layout Considerations

Layout is straightforward if you use the Gerber files on page 21 as a reference. Notice that the input voltage feed to the SC900 is on the bottom of the board and vias connect this voltage track to the top of the board and then to the SC900 itself. The input bypass can be one 4.7 $\mu$ F capacitor, two 3.3 $\mu$ F capacitors, three 2.2 $\mu$ F capacitors or five 1 $\mu$ F capacitors. The determining factor is how much copper is available on the input voltage feed track and how much room is available. If the input

voltage track is very thin, then use five 1 $\mu$ F capacitors placed very close to the input pins of the SC900. If the input track is fairly thick, then you can use a single 4.7 $\mu$ F capacitor at the beginning of the voltage feed track since a wider track has less inductance per inch. The SC900EVb has five 1 $\mu$ F capacitors, but these can be replaced with one 4.7 $\mu$ F in place of C1 and opens in place of C9, C14, C15, and C16 (see page 20 for details).

#### LDO Reset Control Logic Table (Defaults are in Bold)

| Register Name           | Register Address | Bit 7                         | Bit 6                       | Bit 5                                       | Bit 4                               | Bit 3             | Bit 2                | Bit 1                    | Bit 0                |     |                      |     |                      |     |
|-------------------------|------------------|-------------------------------|-----------------------------|---------------------------------------------|-------------------------------------|-------------------|----------------------|--------------------------|----------------------|-----|----------------------|-----|----------------------|-----|
| LDO A                   | 0x00             | X                             | X                           | Active Shutdown<br>1 = <b>ON</b><br>0 = OFF | LDO Output Voltage Codes<br>Table A |                   |                      |                          |                      |     |                      |     |                      |     |
| LDO B                   | 0x01             |                               |                             |                                             |                                     |                   |                      |                          |                      |     |                      |     |                      |     |
| LDO C                   | 0x02             |                               |                             |                                             |                                     |                   |                      |                          |                      |     |                      |     |                      |     |
| LDO D                   | 0x03             |                               |                             |                                             |                                     |                   |                      |                          |                      |     |                      |     |                      |     |
| LDO E                   | 0x04             |                               |                             |                                             |                                     |                   |                      |                          |                      |     |                      |     |                      |     |
| LDO Reset Control       | 0x05             | LDOPGD Pin Reset Polarity Bit | ARST Pin Reset Polarity Bit | LDOPGD Monitor Logic Bits                   |                                     | LDOPGD Delay Bits |                      | LDO (A) Reset Delay Bits |                      |     |                      |     |                      |     |
| On/Off Control Register | 0x06             | X                             | X                           | X                                           | ON/OFF Control LDO E                |                   | ON/OFF Control LDO D |                          | ON/OFF Control LDO C |     | ON/OFF Control LDO B |     | ON/OFF Control LDO A |     |
|                         |                  |                               |                             |                                             | 1                                   | 0                 | 1                    | 0                        | 1                    | 0   | 1                    | 0   | 1                    | 0   |
|                         |                  |                               |                             |                                             | ON                                  | OFF               | ON                   | OFF                      | ON                   | OFF | ON                   | OFF | ON                   | OFF |

#### LDO Reset Control Logic Table (Defaults are in Bold)

| Bit 7               | Result                                            | Bit 6             | Result                                       | Bit 5                | Bit 4 | Result                       | Bit 3 | Bit 2      | Result       | Bit 1    | Bit 0    | Result       |
|---------------------|---------------------------------------------------|-------------------|----------------------------------------------|----------------------|-------|------------------------------|-------|------------|--------------|----------|----------|--------------|
| LDOPGD Pin Polarity |                                                   | ARST Pin Polarity |                                              | LDOPGD Monitor Logic |       | LDOPGD Delay                 |       | ARST Delay |              |          |          |              |
| 0                   | High: Power Fail<br>Low: Power Good               | 0                 | High: Reset<br>Low: Power Good               | 0                    | 0     | <b>LDOs A,C,D&amp;E Good</b> | 0     | 0          | 150ms        | 0        | 0        | 150ms        |
| 1                   | <b>High: Power Good</b><br><b>Low: Power Fail</b> | 1                 | <b>High: Power Good</b><br><b>Low: Reset</b> | 0                    | 1     | LDO E Good                   | 0     | 1          | <b>100ms</b> | 0        | 1        | 50ms         |
|                     |                                                   |                   |                                              | 1                    | 0     | LDO C Good                   | 1     | 0          | 50ms         | <b>1</b> | <b>0</b> | <b>100ms</b> |
|                     |                                                   |                   |                                              | 1                    | 1     | LDO D Good                   | 1     | 1          | 0ms          | 1        | 1        | 0ms          |

#### Notes:

Digital outputs are powered from INB, additionally LDOB must be on for operation of LDOPGD and ARST.

#### SC900 Slave Address:

| DEVICE TYPE IDENTIFIER |   |   |   |   |   | DEVICE ADDRESS | R/W |
|------------------------|---|---|---|---|---|----------------|-----|
| 0                      | 0 | 0 | 1 | 0 | 0 | A0             | X   |

## POWER MANAGEMENT

### Applications Information (Cont.)

#### Output Voltage Code Bits:

A 5-bit linear DAC controls the output voltage of each LDO. The DAC and error-amp gain are scaled so that the LSB size at the output is 50mV. Output voltage can be set by writing the proper code to the desired LDO register. See Table A for the bitcodes and their corresponding voltages.

**Table A - LDO Output Voltage Control Settings**

| Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | LDO Output Voltage |
|-------|-------|-------|-------|-------|--------------------|
| 0     | 0     | 0     | 0     | 0     | 1.45V              |
| 0     | 0     | 0     | 0     | 1     | 1.50V              |
| 0     | 0     | 0     | 1     | 0     | 1.55V              |
| 0     | 0     | 0     | 1     | 1     | 1.60V              |
| 0     | 0     | 1     | 0     | 0     | 1.65V              |
| -     | -     | -     | -     | -     | -                  |
| -     | -     | -     | -     | -     | -                  |
| 1     | 1     | 1     | 1     | 0     | 2.95V              |
| 1     | 1     | 1     | 1     | 1     | 3.00V              |

### Using the I<sup>2</sup>C Interface

The SC900 is a read-write slave-mode I<sup>2</sup>C device and complies with the Philips I<sup>2</sup>C standard Version 2.1 dated January 2000. The SC900 has six user-accessible internal 8-bit registers. The I<sup>2</sup>C interface has been designed for program flexibility, in that once the slave address has been sent to the SC900 enabling it to be a slave transmitter/receiver, any register can be written or read from independent of each other. While there is no auto increment/decrement capability in the SC900 I<sup>2</sup>C logic, a tight software loop can be designed to randomly access the next register independent of which register you begin accessing. The start and stop commands frame the data-packet and the repeat start condition is allowed if necessary.

#### SC900 Limitations to the I<sup>2</sup>C Specifications

Seven-bit addressing is required for communicating with the SC900; ten-bit addressing is not allowed. Any general call address will be ignored by the SC900. Note that the SC900 is not CBUS compatible. Finally, the SC900 can operate in standard mode (100kbit/s) or fast mode (400kbit/s).

## POWER MANAGEMENT

### Applications Information (Cont.)

#### Supported Formats

##### Direct Format - Write

The simplest format for an I<sup>2</sup>C write is the direct format. After the start condition [S], the slave address is sent, followed by an eighth bit indicating a write. The SC900 I<sup>2</sup>C then acknowledges that it is being addressed, and the master responds with an 8-bit data byte consisting of the register address. The slave acknowledges and the master sends the appropriate 8-bit data byte. Once again the slave acknowledges and the master terminates the transfer with the stop condition [P].

##### I<sup>2</sup>C Direct Format - Write

| S | Slave Address | W | A | Register Address | A | Data | A | P |
|---|---------------|---|---|------------------|---|------|---|---|
|---|---------------|---|---|------------------|---|------|---|---|

S : Start Condition  
 W: Write = '0'  
 A : Acknowledge (sent by slave)  
 Sr: Repeated Start Condition  
 P : Stop Condition

Slave Address : 7 bit  
 Register Address : 8 bit  
 Data : 8 Bit

##### Combined Format - Read

After the start condition [S], the slave address is sent, followed by an eighth bit indicating a write. The SC900 I<sup>2</sup>C then acknowledges that it is being addressed, and the master responds with an 8-bit data byte consisting of the register address. The slave acknowledges and the master sends the repeated start condition [Sr]. Once again the slave address is sent, followed by an eighth bit indicating a read. The slave responds with an acknowledge and the previously addressed 8-bit data byte. The master then sends a non-acknowledge (NACK). Finally, the master terminates the transfer with the stop condition [P].

##### I<sup>2</sup>C Combined Format - Read

| S | Slave Address | W | A | Register Address | A | Sr | Slave Address | R | A | Data | B | P |
|---|---------------|---|---|------------------|---|----|---------------|---|---|------|---|---|
|---|---------------|---|---|------------------|---|----|---------------|---|---|------|---|---|

S : Start Condition  
 W: Write = '0'  
 R : Read = '1'  
 A : Acknowledge (Sent by Slave)  
 B : Acknowledge (Sent by Master)  
 Sr: Repeated Start Condition  
 P : Stop Condition

Slave Address : 7 bit  
 Register Address : 8 bit  
 Data : 8 Bit

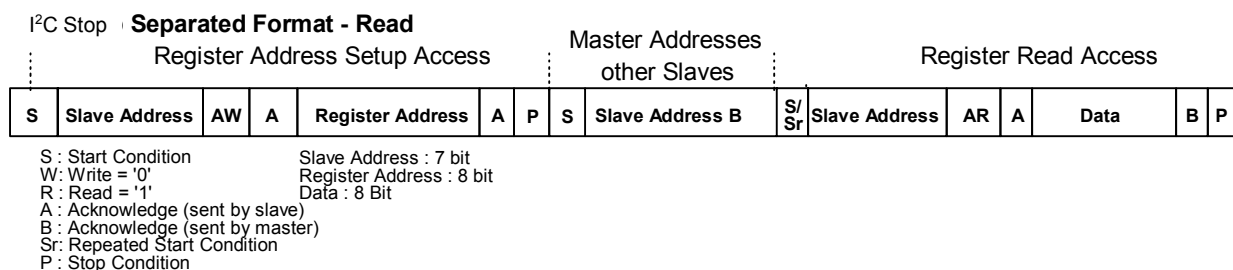
## POWER MANAGEMENT

### Applications Information (Cont.)

#### Stop Separated Reads

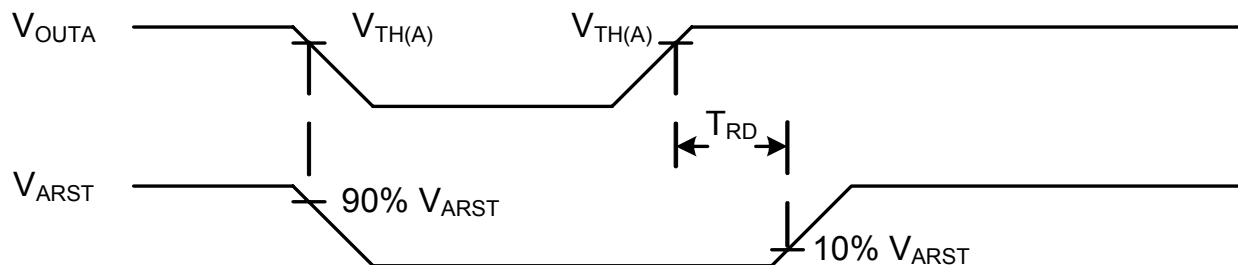
Another read format is available which is, in effect, an extension of the combined format read. This format allows a master to set up the register address pointer for a read and return to that slave some time later to read the data.

After the start condition [S], the slave address is sent, followed by a write. The SC900 I<sup>2</sup>C then acknowledges that it is being addressed, and the master responds with the 8-bit register address. The master then sends a stop or restart condition, and may address another slave. Some time later the master sends a start or restart condition, and a valid slave address is sent, followed by a read. The SC900 I<sup>2</sup>C then acknowledges and returns the data at the register address location that had previously been set up.

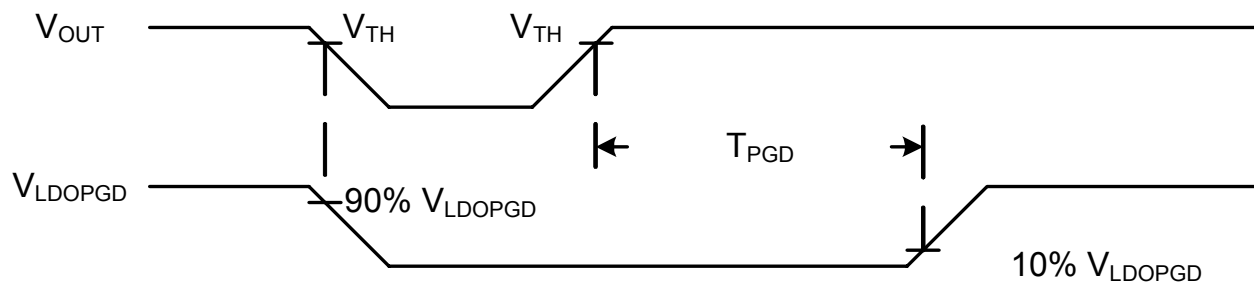


### ARST & LDOPGD Timing

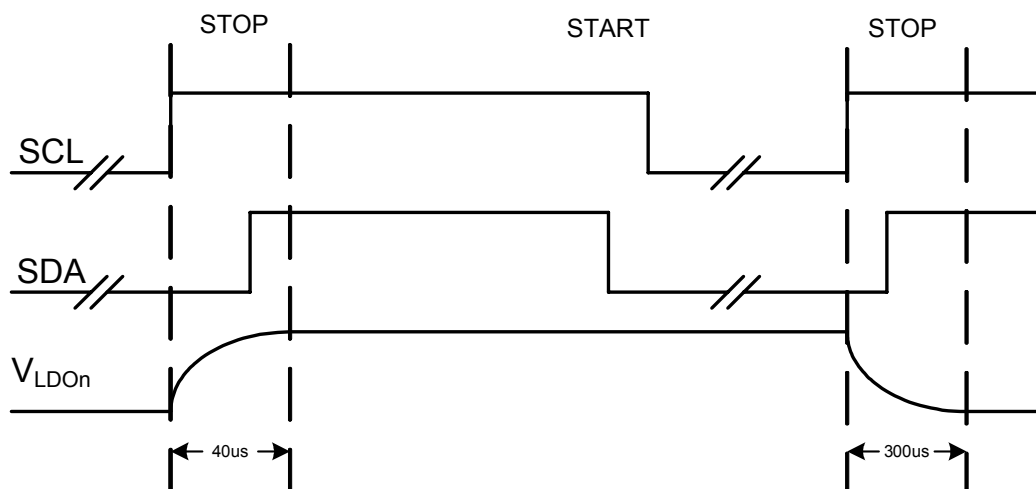
LDO A:



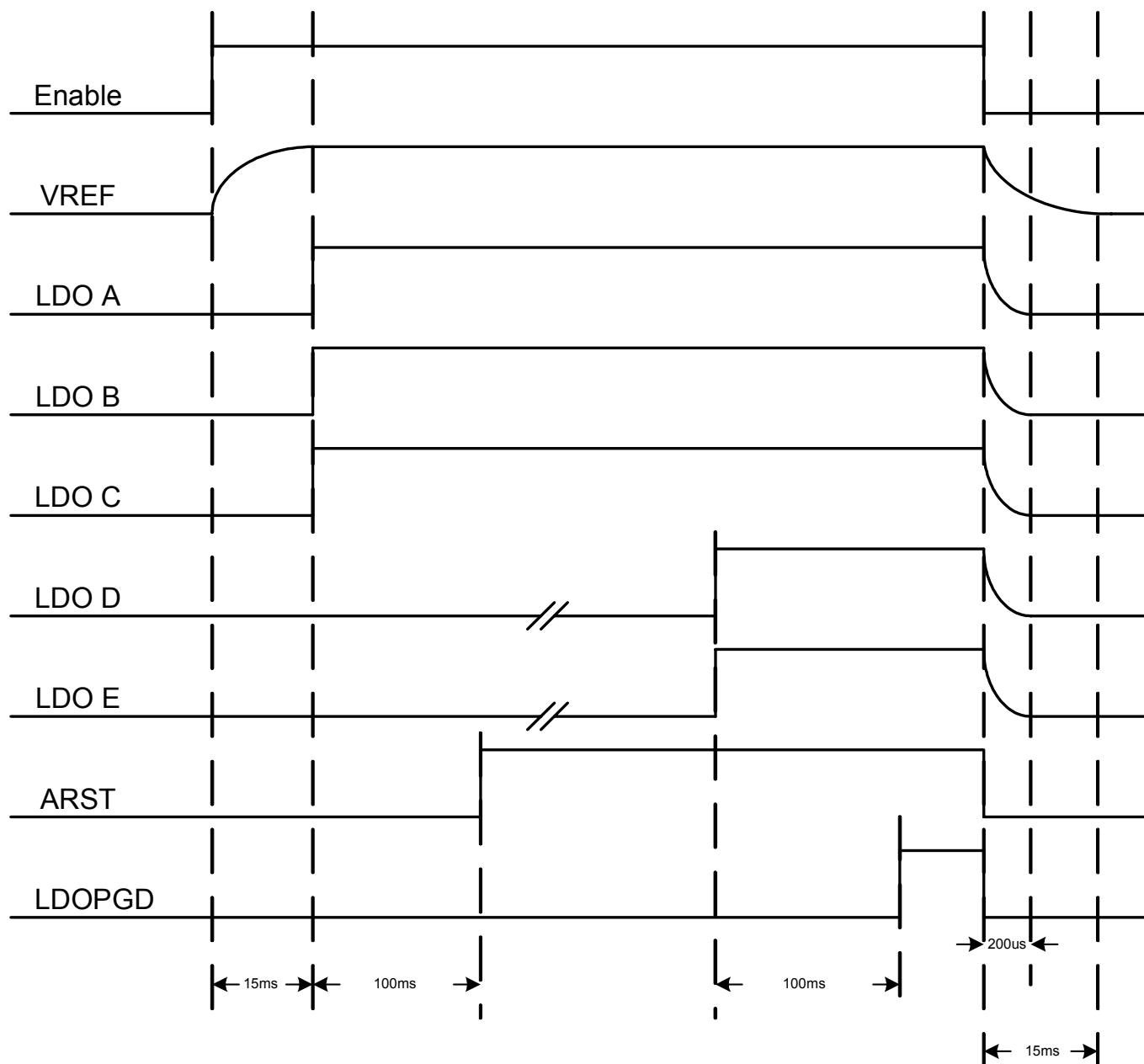
LDO A, C, D, & E:

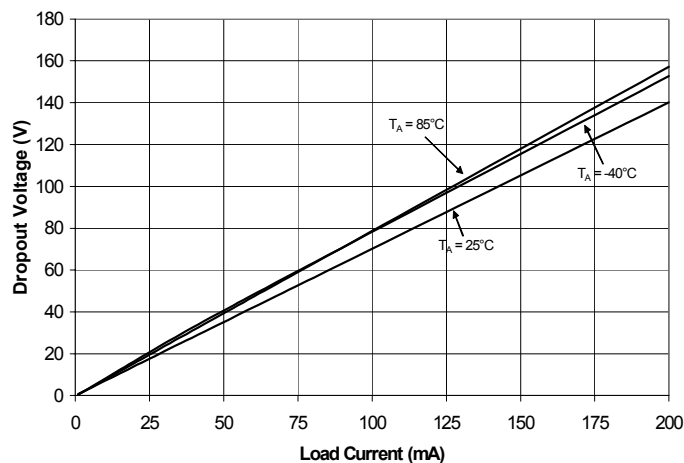
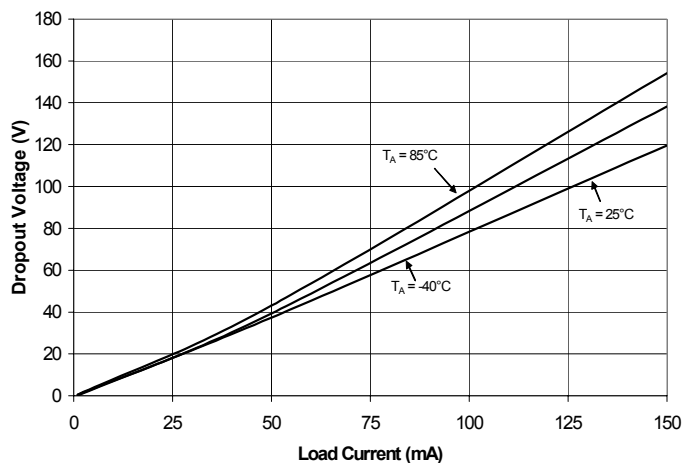
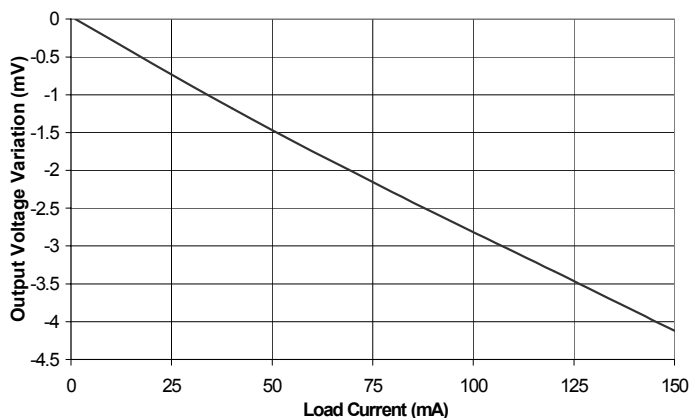
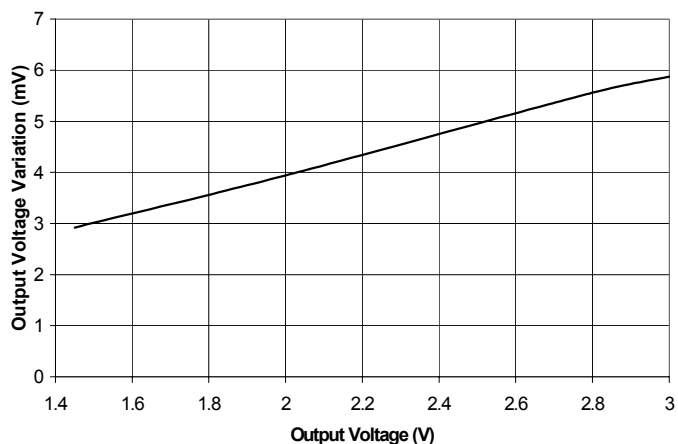
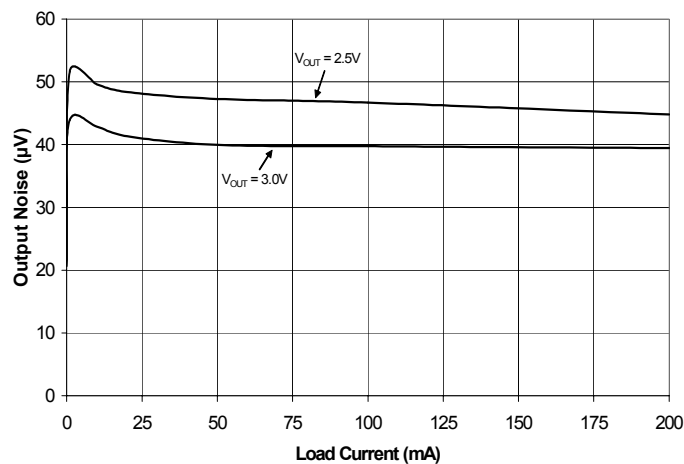


### LDO On/Off Control via the I<sup>2</sup>C Interface



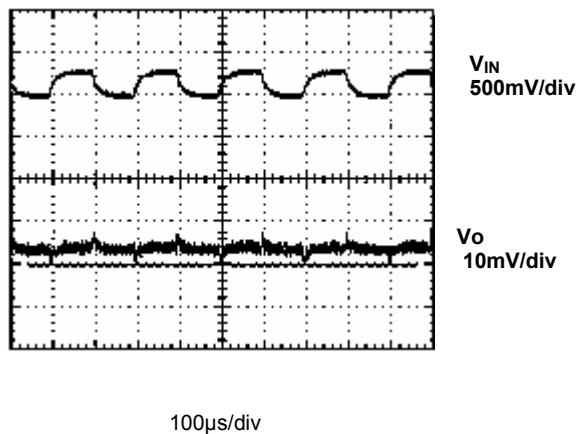
### Default Start-Up, Shut-Down Timing Diagram



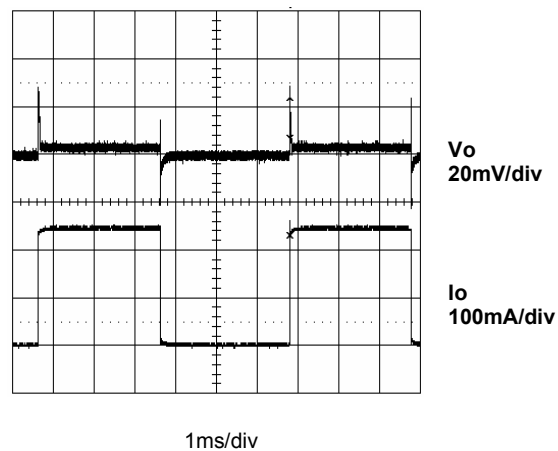
**POWER MANAGEMENT**
**Typical Characteristics**
**Dropout Voltage (LDOA)**

**Dropout Voltage (LDOB-E)**

**Load Regulation (LDOA-E)**
 $T_A = 25^\circ\text{C}, V_{IN} = 3.7\text{V}$ 

**Line Regulation (LDOA-E)**
 $V_{IN(MIN)} < V_{IN} < 5.5\text{V}$ 

**Output Noise vs. Load Current (LDOA-E)**


**POWER MANAGEMENT**
**Typical Characteristics**

**Line Transient**  
 $V_{IN} = 3.7V$ ,  $I_O = 100mA$

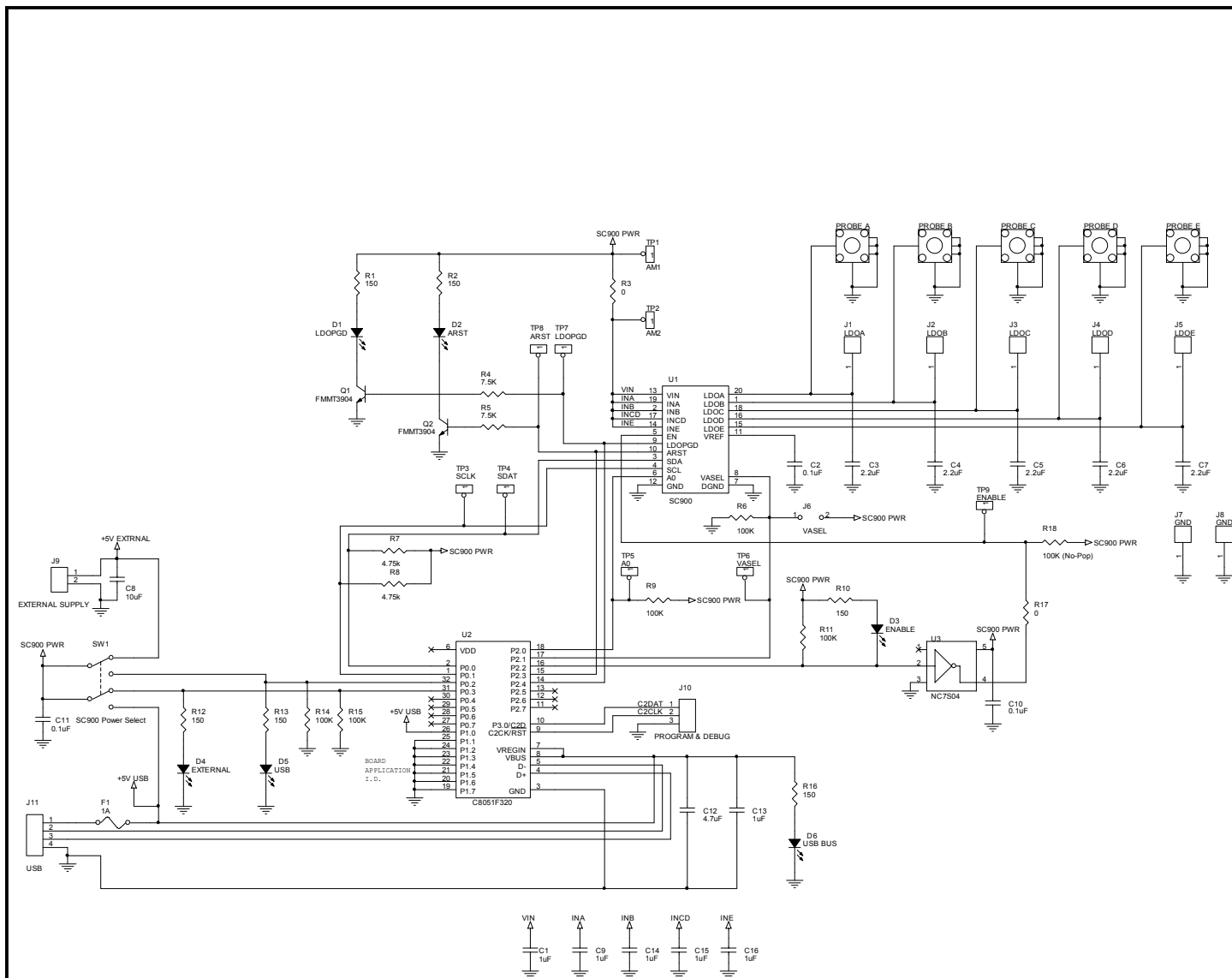


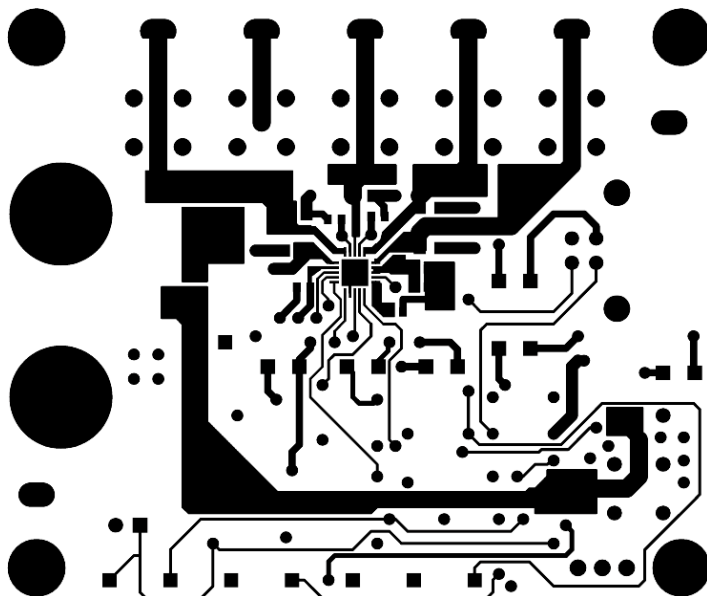
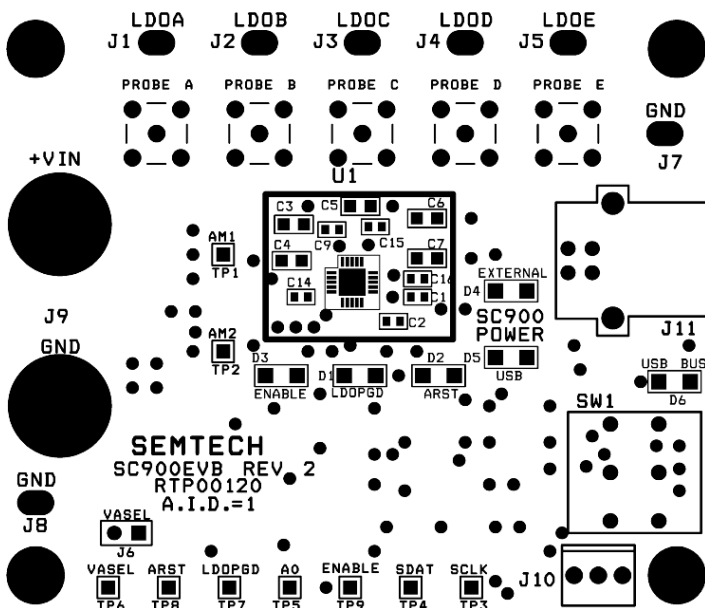
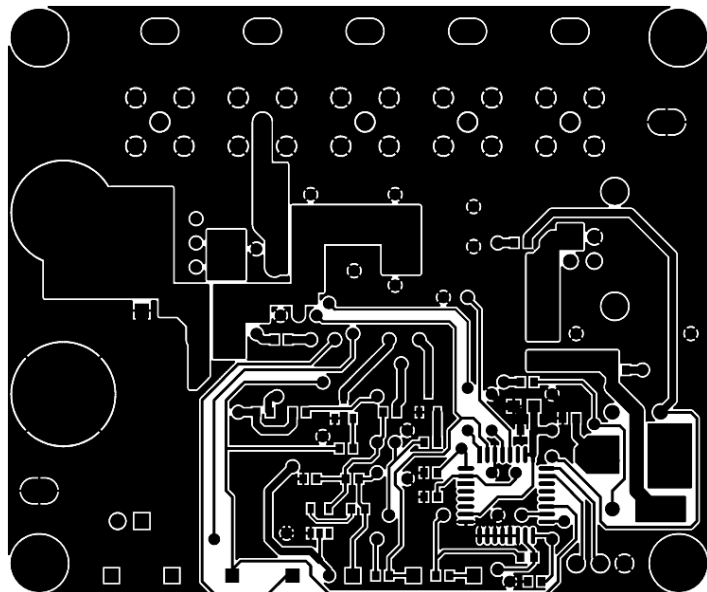
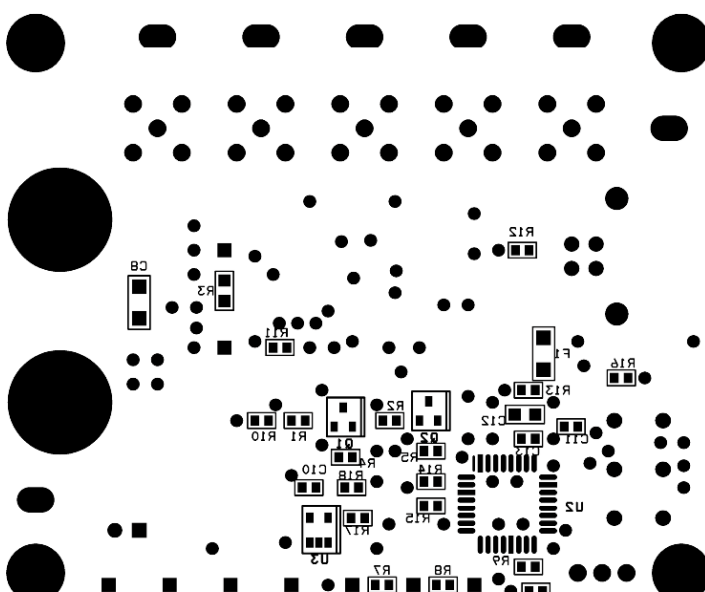
**Load Transient (LDOA-E)**  
 $V_{IN} = 3.7V$ ,  $I_O = 10mA$  to  $150mA$  step

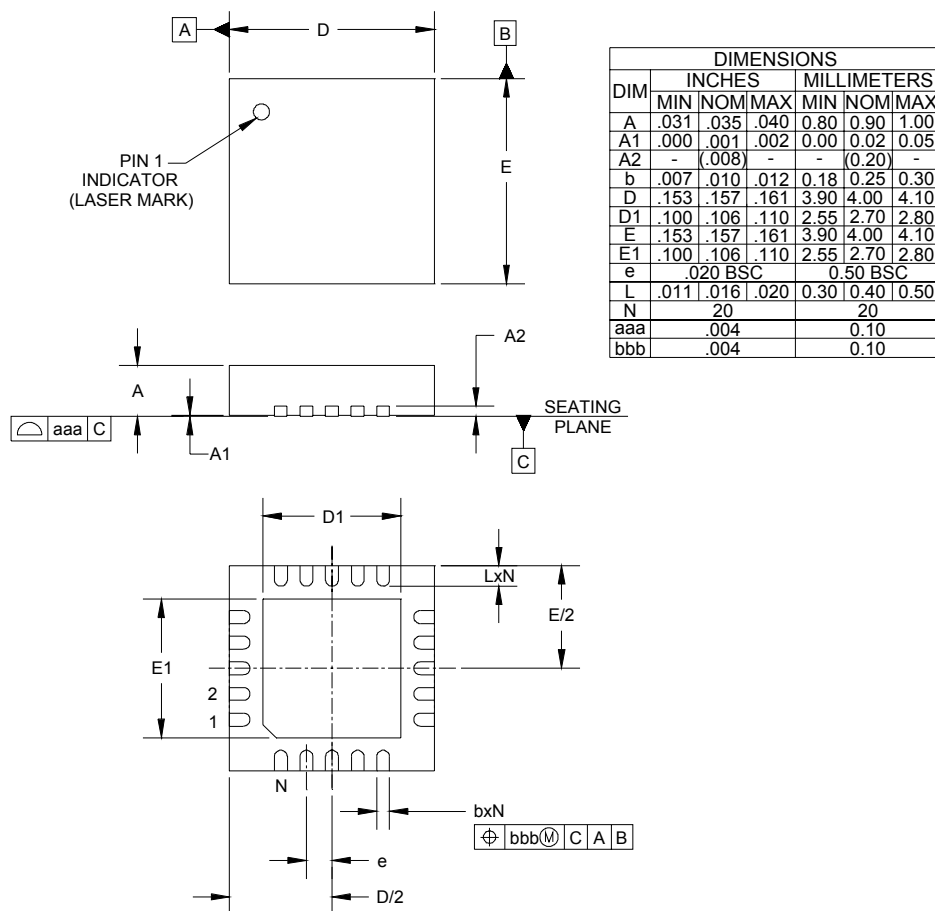


## POWER MANAGEMENT

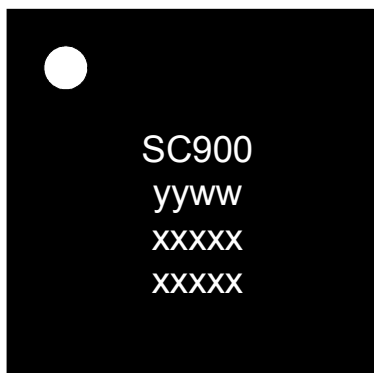
### Evaluation Board



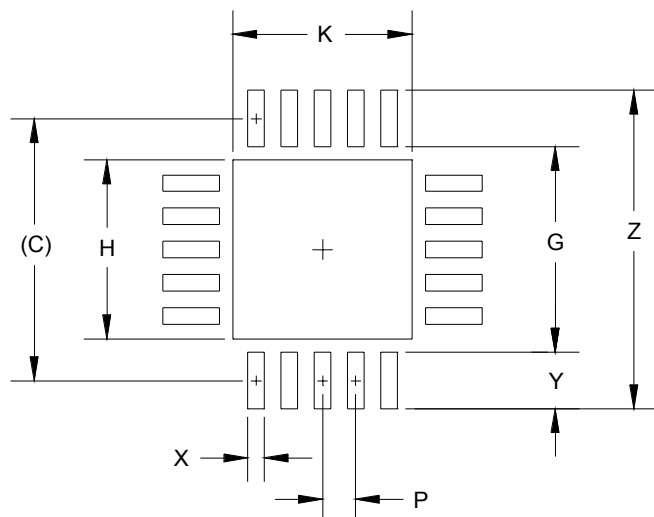
**POWER MANAGEMENT**
**Evaluation Board Gerbers**
**Top Gerber**

**Top Silk Screen Gerber**

**Bottom Gerber**

**Bottom Silk Screen Gerber**


**POWER MANAGEMENT**
**Outline Drawing - MLPQ-20L 4 x 4**

**NOTES:**

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

**Marking Information**


yy = two digit year of manufacture  
ww = two digit week of manufacture  
xxxxx = lot number

**POWER MANAGEMENT**
**Land Pattern - MLPQ-20L 4 x 4**


| DIMENSIONS |        |             |
|------------|--------|-------------|
| DIM        | INCHES | MILLIMETERS |
| C          | (.155) | (3.95)      |
| G          | .122   | 3.10        |
| H          | .106   | 2.70        |
| K          | .106   | 2.70        |
| P          | .021   | 0.50        |
| X          | .010   | 0.25        |
| Y          | .033   | 0.85        |
| Z          | .189   | 4.80        |

**NOTES:**

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.  
CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR  
COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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