

### TEST AND MEASUREMENT PRODUCTS

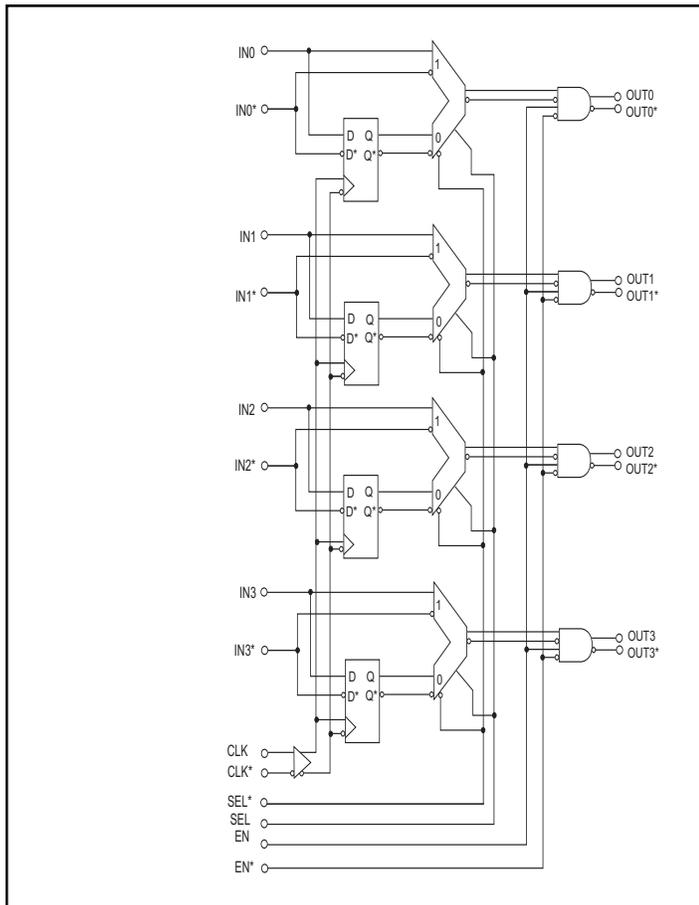
#### Description

The SK4429 is an extremely fast, stable and accurate low skew quad buffer or cable driver / receiver. It can asynchronously pass four distinct signals, or it can resynchronize them to a common clock. In addition, all four outputs may be asynchronously enabled or disabled. All of the D flip-flops are triggered on the rising edge of the CLK input. It is also capable of receiving inputs of any technology or voltage level.

The SK4429 uses 50Ω outputs with sink/source capability, and is optimized for applications that require:

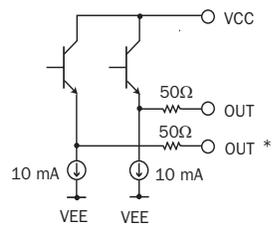
- Point to point, double terminated, timing critical lines
- Point to point, series terminated, timing critical lines

#### Functional Block Diagram

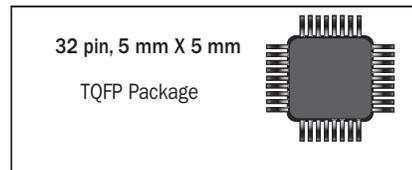


#### Features

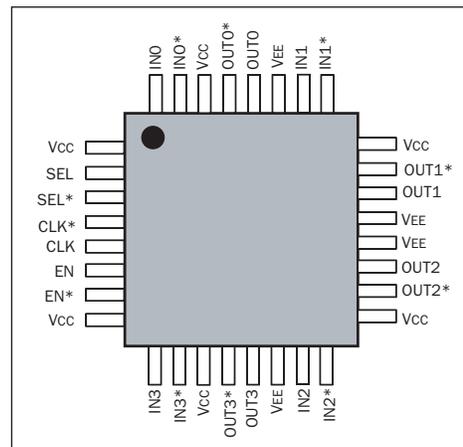
- Quad Buffer/Receiver
- 3 GHz Fmax
- Anything to PECL Translation
- Available in 32 lead, 5mm X5mm, TQFP Package

Input Options	Output Options
Open	50Ω Source / Sink
$IN<0 - 3>$ 	
$IN<0 - 3>^*$ 	

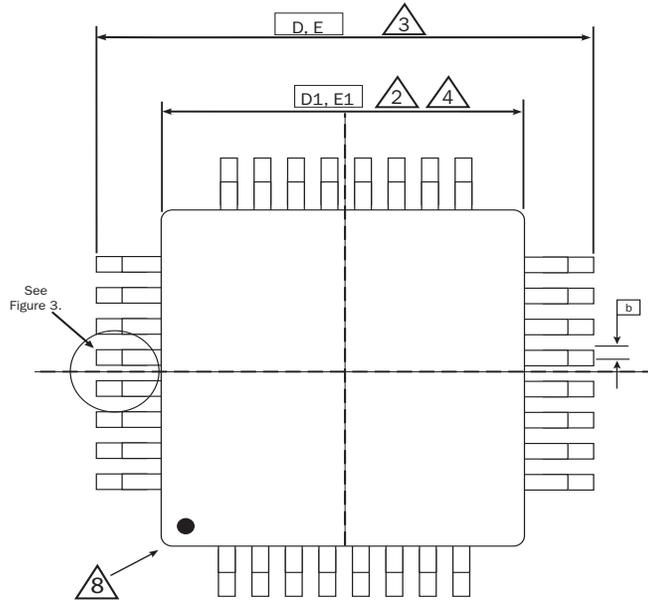
#### Package Information



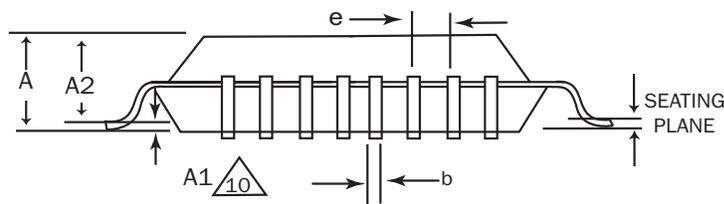
#### Pin Description



**32 Pin, 5mm x 5mm TQFP Package**



Top View



Side View

### 32 Pin, 5mm x 5mm TQFP Package

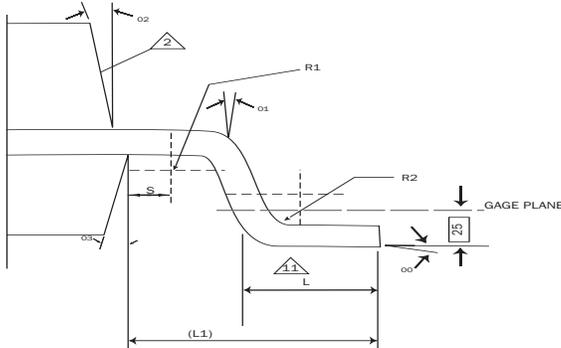


Figure 1.

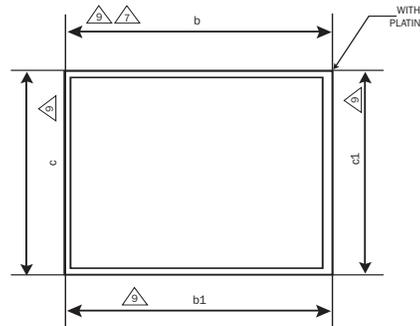


Figure 2.

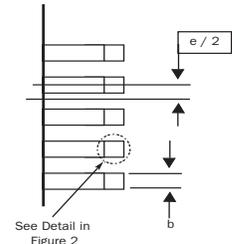


Figure 3.

1. All dimensions and tolerancing conforms to ANSI Y14.5M-1982.
2. The top package body size may be smaller than the bottom package body size by as much as 0.15 mm.
3. To be determined at seating plane.
4. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
5. Details of Pin 1 identifier optional, but must be located within the zone indicated.
6. All dimensions are in millimeters.
7. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
8. Exact shape of each corner is optional.
9. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
10. A1 is defined as the distance from the seating plane to the lowest point of the package body.

JEDEC Variation					
All Dimensions in Millimeters					
Symbol	MIN	NOM	MAX	Note	Comments
A	1.00	1.10	1.20		Package Stand Off Height
A1	0.05	0.10	0.15		Air Gap
A2	0.95	1.00	1.05		Package Body Thickness
D	7.00 BSC			3	
D1	5.00 BSC			4, 2	Package Body Length
E	7.00 BSC			3	
E1	5.00 BSC			4, 2	Package Body Width
N	32				Lead Count
e	0.50 BSC				Lead Pitch
b	0.17	0.22	0.27	7	Lead Thickness
b1	0.17	0.20	0.23		
R1	0.08	-	-		
R2	0.08	-	0.20		
O0	0°	3.5°	7°		
O1	0°	-	-		
O2	11°	12°	13°		
O3	11°	12°	13°		
S	0.20	-	-		
c	0.09	-	0.20		
c1	0.09	-	0.16		
L	0.45	0.60	0.75		
L1	1.00 REF				
aaa	0.20				
bbb	0.20				
ccc	0.08				
ddd	0.08				

**TEST AND MEASUREMENT PRODUCTS**
**Absolute Maximum Ratings\***

Symbol	Parameter	Value	Unit
$V_{EE}$	Power Supply ( $V_{CC} = 0V$ )	-8.0 to 0	V
$V_{CC}$	Power Supply ( $V_{EE} = 0V$ )	+8.0 to 0	V
$V_I$	Input Voltage	$V_{CC} \geq V_I \geq V_{EE}$	V
$I_{OUT}$	Output Current Continuous Surge	50 100	mA mA
$T_{stg}$	Storage Temperature	-65 to +150	$^{\circ}C$
$T_{sol}$	Solder Temperature (<2 to 3 seconds: 245 $^{\circ}C$ desired)	265	$^{\circ}C$

\* Maximum Ratings are those values beyond which damage to the device may occur.

Note 1: Device is ESD sensitive and requires protective handling.

### TEST AND MEASUREMENT PRODUCTS

#### DC Characteristics

(V<sub>CC</sub> = 2.0V to 3.6V; V<sub>EE</sub> = -3.6V to -3.0V; T<sub>A</sub> = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High	V <sub>IH</sub>	V <sub>EE</sub> + 2.0		V <sub>CC</sub>	V
Input Low	V <sub>IL</sub>	V <sub>EE</sub>		V <sub>CC</sub> - 0.2	V
(IN - IN*, CLK - CLK*, EN - EN*, SEL - SEL*) Differential Input Voltage	V <sub>IH</sub> - V <sub>IL</sub>	0.2		4.3	V
Timing Inputs (CLK / CLK*)					
Input High Current	I <sub>IH</sub>	-5.0	+8.0	+25	μA
Input Low Current	I <sub>IL</sub>	-1	<0.5	+1	μA
Timing Inputs (IN / IN*)					
Input High Current, Input Low Current	I <sub>IH</sub> , I <sub>IL</sub>	-20	<40	80	μA
Functional Inputs (EN / EN*, SEL / SEL*) Input Current					
	I <sub>IH</sub> , I <sub>IL</sub>	-500	<200	+500	μA
Outputs					
Digital Output Voltage	OUT - OUT*	600	780		mV
Output Common Mode Range	(OUT + OUT*) / 2	V <sub>CC</sub> - 1.5	V <sub>CC</sub> - 1.3	V <sub>CC</sub> - 1.1	V
Internal Current Source	I <sub>SINK</sub>	8.0	10.5	13.5	mA
Output Impedance	R <sub>OUT</sub>	40	50	60	Ω
Power Supply					
Power Supply Current	I <sub>EE</sub>		170	235	mA

DC Test Conditions: Outputs unterminated.

#### AC Characteristics

(V<sub>CC</sub> = 2.0V to 3.6V; V<sub>EE</sub> = -3.6V to -3.0V; T<sub>A</sub> = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay					
IN[0:3] to OUT[0:3] (SEL = 1)	T <sub>pd</sub>	200	350	550	ps
CLK to OUT[0:3] (SEL = 0)	T <sub>pd</sub>	430	580	780	ps
SEL to OUT [0:3]	T <sub>pd</sub>	300	450	650	ps
EN to OUT [0:3]	T <sub>pd</sub>	250	350	600	ps
Channel to Channel Skew			15	40	ps
Maximum Operating Frequency <sup>1</sup>	F <sub>max</sub>	3			GHz
Minimum Pulse Width <sup>1</sup>	PW min	250			ps
IN to CLK					
Set Up Time	T <sub>s</sub>	120			ps
Hold Time	T <sub>h</sub>	120			ps
Output Rise and Fall Times (20% / 80%) <sup>1</sup>	T <sub>r</sub> / T <sub>f</sub>		125	165	ps
Temperature Coefficient <sup>1</sup>	ΔT <sub>pd</sub> / ΔT		<1		ps / °C

AC Test Conditions: Outputs terminated with 50Ω to V<sub>CC</sub> - 2V

Note 1: Guaranteed by characterization. Not production tested.

**TEST AND MEASUREMENT PRODUCTS****Ordering Information**

Ordering Code	Package ID
SK4429ATF	32 Pin - TQFP 5 X 5 mm
S4429ATF-T	Tape and Reel

*Notes:*

1. For Tape and Reel information, see TMD Part Ordering Information Data Sheet.

**Application Notes**

AN1001 - EPIC Family Product Line

AN1003 - Termination Techniques for ECL / LVECL  
PECL / LVPECL Devices

AN1004 - Interfacing Between LVDS and  
ECL / LVECL / PECL / LVPECL

**Contact Information**

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