Edge846
Pin Electronics Driver, Window Comparator, and Switch Matrix

TEST AND MEASUREMENT PRODUCTS

Description

The Edge846 is an integrated trinary driver, window comparator, and switch matrix pin electronics solution manufactured in a wide voltage CMOS process. It is designed for automatic test equipment and instrumentation where cost, functional density, and power are all at a premium.

The tristatable driver is capable of generating 3 levels - one for a logic high, one for a logic low, and one for either a termination voltage or a special programming voltage.

The on-board window comparator effectively determines whether the DUT is in a high, low, or intermediate state.

The switches are included to allow such functions as PMU, pull-up, and pull-down connections.

The Edge846 is intended to offer an extremely low leakage, low cost, low power, highly integrated, per pin solution for 50 MHz and below pin electronics applications.

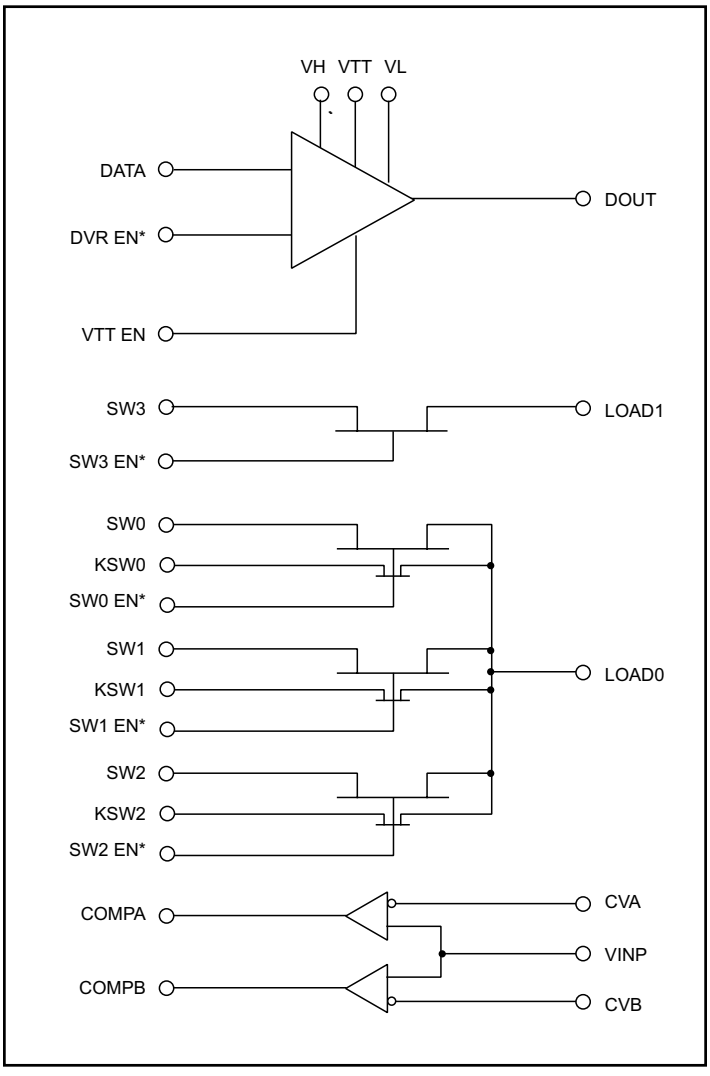
Applications

- Low Cost ATE

Features

- 50 MHz Operation
- 18 V DUT I/O Range
- Programmable Output Levels
- Programmable Input Thresholds
- Three Level Driver
- Extremely Low Leakage Currents (<5 nA)
- Small Footprint (32 Pin, 7 mm X 7 mm, TQFP Package)

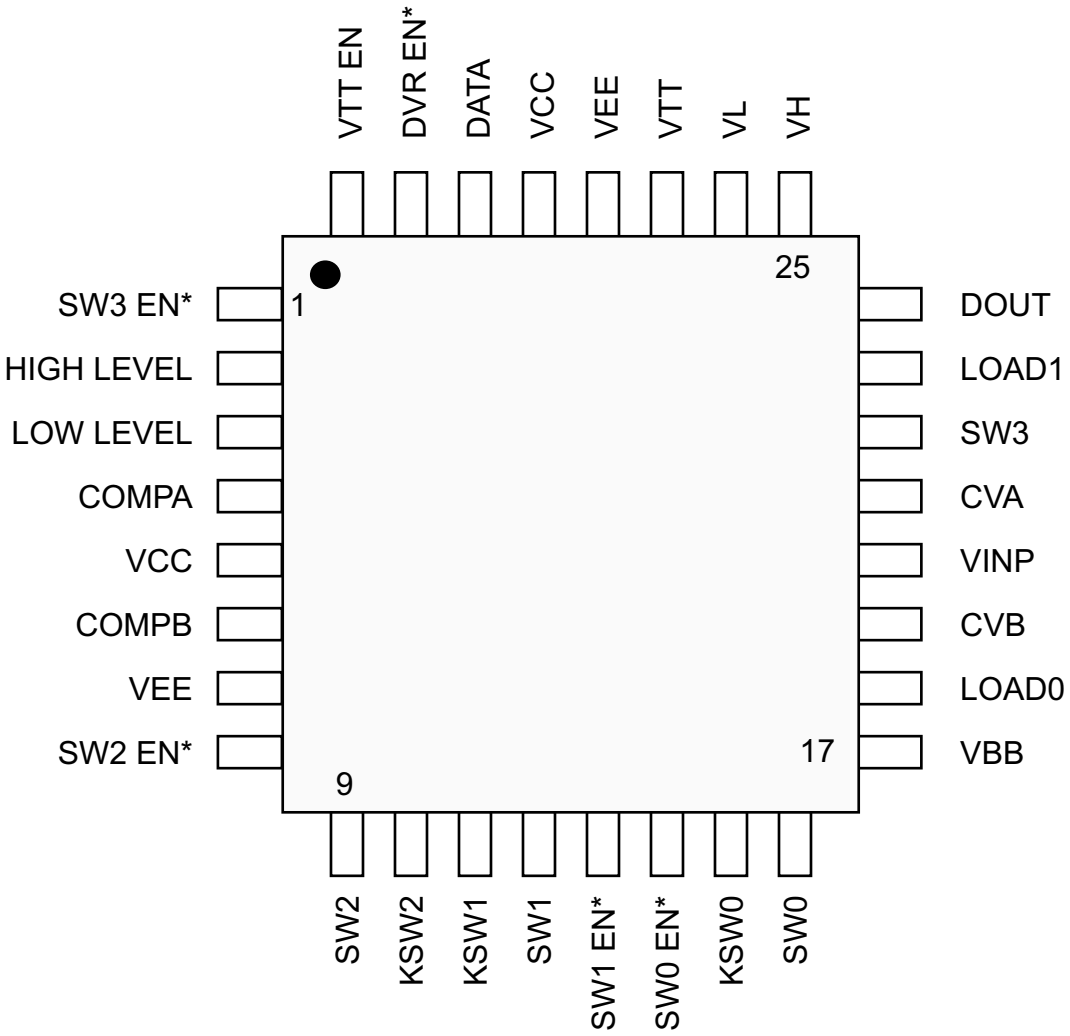
Functional Block Diagram



PIN Description

Pin #	Pin Name	Description
Driver		
30	DATA	Digital input that determines the high/low status of the driver when it is enabled.
31	DVR EN*	Digital input that enables and disables the driver, or places the driver in the VTT state.
32	VTT EN	Digital input that determines whether DVR EN* places the driver in a high impedance state or actively drives to the VTT level.
24	DOUT	Driver output.
25, 26, 27	VH, VL, VTT	Unbuffered inputs that set the voltage level of a logical 1, 0, or VTT at the driver output.
17	VBB	Analog input pin which establishes the threshold for all digital single ended input signals.
Comparator		
20	VINP	Analog window comparator input.
21, 19	CVA, CVB	Analog DC comparator inputs that set the threshold levels for the window comparator.
4, 6	COMPA, COMPB	Digital comparator outputs.
3 2	LOW LEVEL HIGH LEVEL	Voltage inputs that establish the digital low and high levels of the comparator outputs.
Switch Matrix		
14, 13 8, 1	SW0 EN*, SW1 EN* SW2 EN*, SW3 EN*	TTL compatible inputs that activate switches 0, 1, 2, and 3.
16, 15 12, 11 9, 10 22	SW0, KSW0 SW1, KSW1 SW2, KSW2 SW3	Switch 0 and its Kelvin sense output. Switch 1 and its Kelvin sense output. Switch 2 and its Kelvin sense output. Switch 3.
18 23	LOAD0 LOAD1	Input pins that connect the DUT to the analog switches.
Power Supplies		
5, 29	VCC	Positive analog power supply.
7, 28	VEE	Negative analog power supply.

PIN Description *(continued)*



Circuit Description

Driver Description

The Edge846 supports three programmable driver levels - high, low, and termination - and high impedance. There are no restrictions between any of these three levels in that all three may vary independently over the entire operating voltage range between VCC and VEE.

The DVR EN*, DATA, and VTT EN pins are digital inputs that control the driver (see Table 1). With DVR EN* low, DATA determines whether the driver will force VH or VL at DOUT. With DVR EN* high, VTT EN* controls whether the driver goes into high impedance or drives VTT.

DVR EN*	VTT EN	DATA	DOUT
1	0	X	HiZ
1	1	X	VTT
0	X	0	VL
0	X	1	VH

Table 1. Driver Truth Table

VH, VL, and VTT

VH, VL, and VTT define the logical "1", "0", and "termination" levels of the driver and can be adjusted anywhere over the range spanned by VCC to VEE. There is no restriction between VH, VL, and VTT, in that they can all vary independently over the entire voltage range determined by the power supply levels.

The VH, VL, and VTT inputs are unbuffered in that they also provide the driver output current, so the sources of these voltages must have ample current drive capability.

While VTT is referred to as the termination voltage, it may also be used as a very high "programming" level on many memory devices.

Driver Output Protection

The Edge846 is designed to operate in a functional testing environment where a controlled impedance (typically 50 Ohms) is maintained between the pin electronics and the DUT. In general, there will be an external resistor at the driver output which series terminates the transmission line to the DUT. In this environment, the driver can withstand a short to any legal DUT voltage for an indefinite amount of time.

In a low impedance application with no additional output series resistance, care must be exercised and systems should be designed to check for this condition and tristate the driver if a short is detected.

The driver does NOT have on-chip short circuit protection or limitation circuitry.

VBB

VBB is an analog input which establishes the threshold for all digital input signals. If DATA, DVR EN*, or VTT EN are more positive than VBB, these inputs are a digital "1". Conversely, if they are more negative than VBB, they are a "0".

All digital inputs are wide voltage comparator inputs, so they are technology independent. By establishing the appropriate VBB level, the Edge846 may be driven by TTL, ECL, CMOS, or any custom level circuitry.

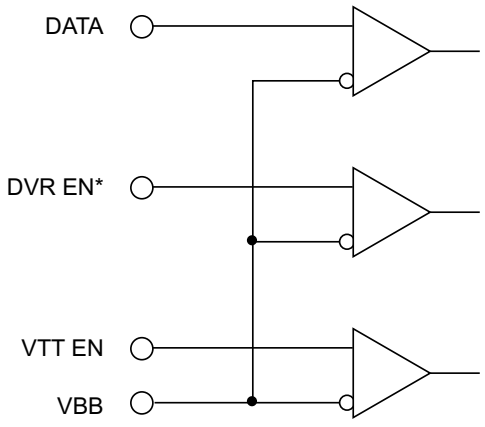


Figure 1. Digital Input Translation Stage

Circuit Description *(continued)*

Receiver Functionality

The Edge846 supports an on-board window comparator. CVB and CVA are high impedance analog inputs which establish the threshold voltages. COMPA and COMPB are the digital outputs which reflect the real time status of VINP. Table 2 summarizes the relationship between the threshold levels, VINP, and the output signals.

VINP	COMPA	COMPB
VINP < CVA VINP > CVA	0 1	X X
VINP < CVB VINP > CVB	X X	0 1

Table 2. Comparator Truth Table

Comparator Outputs

The digital outputs of the comparator are standard CMOS outputs that are also adjustable. Input pins LOW LEVEL and HIGH LEVEL establish the logic 0 and 1 levels respectively. In normal operation, LOW LEVEL would be connected to ground and HIGH LEVEL would be connected to a system VDD supply, producing CMOS digital swings at the output.

However, the comparator outputs are technology independent in that they can drive PECL, 3V CMOS, ECL, LVCMOS, GTL, and custom levels by varying LOW LEVEL and HIGH LEVEL. For example, should a 3V swing be desired, HIGH LEVEL could be connected to a 3.0V power supply.

Notice that HIGH LEVEL and LOW LEVEL provide both the voltage level and the current for the comparator outputs. HIGH LEVEL and LOW LEVEL may be varied between +5V and -2V.

Analog Switches

The Edge846 provides a total of 7 analog switches. Individual switches vary in both their on resistance, their on / off time, and their DC current rating (see Tables 4 and 5).

Like the driver digital inputs, the switch matrix control inputs SW0-3 EN* are technology independent as VBB determines their threshold level. The switch control is documented in Table 3.

Control Inputs	Status
SW0 EN* = 1 SW0 EN* = 0	SW0 and KSW0 disconnected SW0 and KSW0 connected
SW1 EN* = 1 SW1 EN* = 0	SW1 and KSW1 disconnected SW1 and KSW1 connected
SW2 EN* = 1 SW2 EN* = 0	SW2 and KSW2 disconnected SW2 and KSW2 connected
SW3 EN* = 1 SW3 EN* = 0	SW3 disconnected SW3 connected

Table 3. Switch Matrix Truth Table

Switch	Rout	On / Off Time	1 DC
Central PMU SW0 KSW0	 30 Ω 1 KΩ	 100 ns 100 ns	 30 mA 1 mA
PPMU SW1 KSW1	 100 Ω 1 KΩ	 100 ns 100 ns	 5 mA 1 mA
Cal Voltage SW2 KSW2	 100 Ω 1 KΩ	 100 ns 100 ns	 5 mA 1 mA
HiZ Voltage SW3	 30 Ω	 10 ns	 30 mA

Table 4. Switch Matrix Characteristics

All switch enable inputs have an internal pull up resistor to VCC. When left floating, these enable pins will be high and the corresponding switches will be open.

	Rout	On / Off Time	1 DC
VH	30 Ω	10 ns	50 mA
VL	30 Ω	10 ns	50 mA
VTT	30 Ω	10 ns	50 mA

Table 5. Switch Characteristics

Circuit Description *(continued)*

Power Supplies

The Edge846 uses two power supplies for circuit operation; VCC and VEE. In order to protect the Edge846 and avoid damaging it, the following power supply requirements must be satisifed at all times:

$$VEE \leq \text{All Inputs} \leq VCC$$

The sequence below can be used as a guideline when operating the Edge846:

Power-On Sequencing	*Power-Off Sequencing*
1. VCC (substrate)	1. Inputs
2. VEE	2. VEE
3. Inputs	3. VCC

The three diode configuration shown in Figure 2 should be used on a once-per-board basis to ensure power supply sequence and fault tolerance.

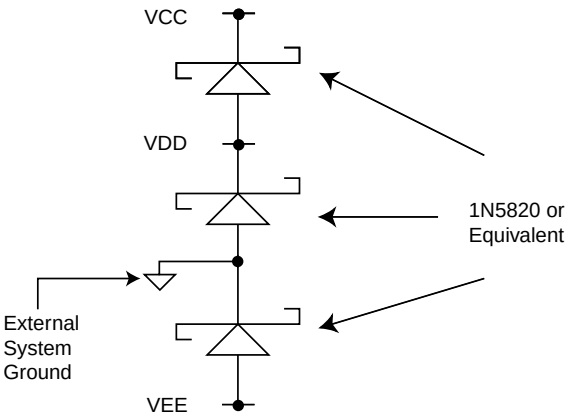


Figure 2. Power Supply Protection Scheme

Warning: It is extremely important that the voltage on any device pin does not exceed the range of VEE –0.5V to VCC +0.5V at any time, either during power up, normal operation, or during power down. Failure to adhere to this requirement could result in latchup of the device, which could be destructive if the system power supplies are capable of supplying large amounts of current. Even if the device is not immediately destroyed, the cumulative damage caused by the stress of repeated latchup may affect device reliability.

Power Supplies Decoupling

A .1 µF capacitor is recommended between VCC and VEE.

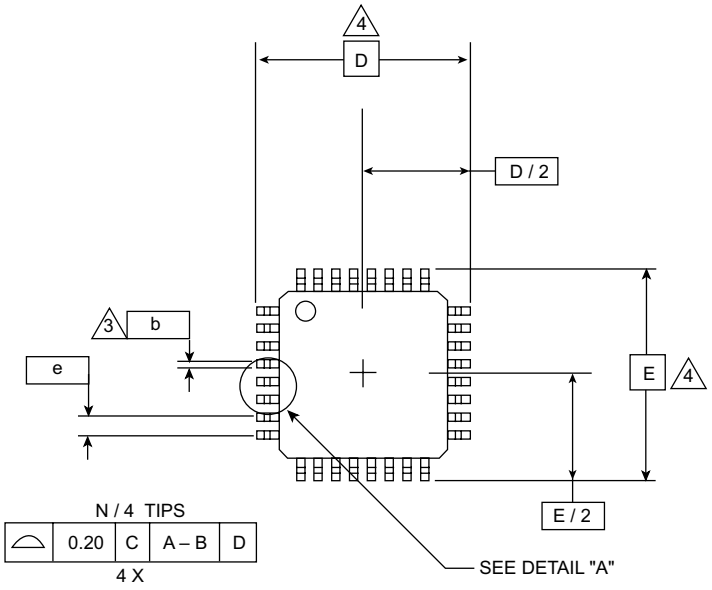
In addition, solid VCC and VEE planes are recommended to provide a low inductance path for the power supply currents. These planes will reduce any inductive supply drops associated with swtiching currents on the power supply pins. If solid planes are not possible, then wide power busses are preferable.

VH, VL, and VTT Decoupling

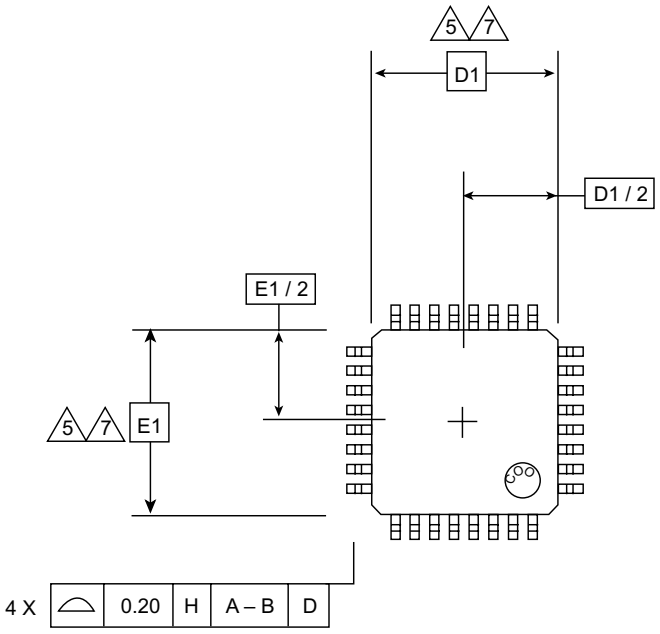
As the VH, VL, and VTT inputs are unbuffered and must supply the driver output current, decoupling capacitors for these inputs are recommended in proportion to the amount of output current the application requires. In general, a surge current of 50 mA (5V swings series terminated with 50 Ohms into a 50 Ohm transmission line) are the maximum dynamic output currents the driver should see. The decoupling capacitors should be able to provide this current for the duration of the round trip time between the pin electronics and the DUT, and then recharge themselves before the next such transition would occur. Once this condition is satisfied, the VH, VL, and VTT supply voltages are more responsible for establishing the DC levels associated with each function and recharging the capacitors, rather than providing the actual dynamic currents required to drive the DUT transmission line.

Ideally, VH, VL, and VTT would each have a dedicated power layer on the PC board for the lowest possible inductance power supply distribution.

TOP VIEW

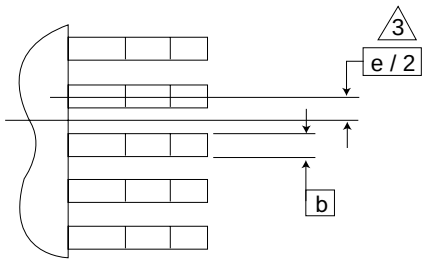


BOTTOM VIEW

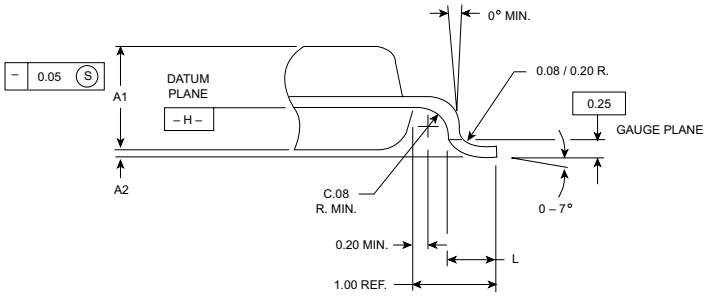


Package Information *(continued)*

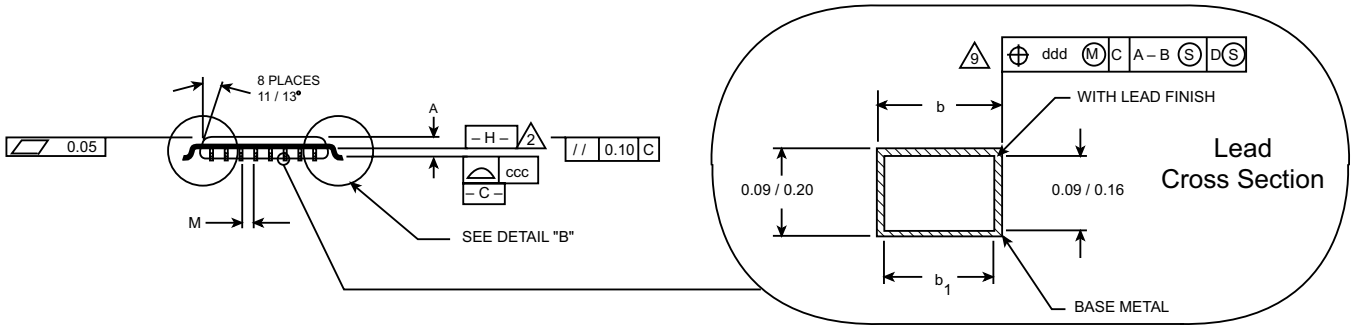
DETAIL "A"



DETAIL "B"



SECTION C–C



Notes:

1. All dimensions and tolerances conform to ANSI Y14.5-1982.
2. Datum plane -H- located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and -D- to be determined at centerline between leads where leads exit plastic body at datum plane -H-.
4. To be determined at seating plane -C-.
5. Dimensions D1 and E1 do not include mold protrusion.
6. “N” is the total # of terminals.
7. These dimensions to be determined at the datum plane -H-.
8. Package top dimensions are smaller than bottom dimensions and top of package will not overhang bottom of package.
9. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
10. Controlling dimension: millimeter.
11. Maximum allowable die thickness to be assembled in this package family is 0.30 millimeters.
12. This outline conforms to JEDEC publication 95, registration MO-136, variations AC, AE, and AF.

	JDEC Variations Dimensions in Millimeters				
Sym	Min	Nom	Max	Note	Comments
A			1.60		Package Stand Off Height
A1	0.05	0.10	0.15		Air Gap
A2	1.35	1.40	1.45		Package Body Thickness
D		9.00 BSC		4	
D1		7.00 BSC		7,8	Package Body Length
E		9.00 BSC		4	
E1		7.00 BSC		7,8	Package Body Width
L	0.45	0.60	0.765		
M	0.15			5	
N		32			Lead Count
e		0.80 BSC			Lead Pitch
b	0.30	0.37	0.45	9	Lead Thickness
b1	0.30	0.35	0.40		
ccc			0.10		
ddd			0.20		

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Positive Analog Power Supply	VCC	11	14	18	V
Negative Analog Power Supply	VEE	–5	–4	0	V
Total Analog Power Supply	VCC – VEE	11		18	V
Ambient Operating Temperature	TA	0		70	˚C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Total Analog Power Supply	VCC – VEE	0		20	V
Positive Analog Power Supply	VCC	0		20	V
Negative Analog Power Supply	VEE	–8		0	V
Analog Input Voltages		VEE – .5		VCC + .5	V
Digital Inputs		VEE – .5		VCC + .5	V
Ambient Operating Temperature	TA	–55		+125	˚C
Storage Temperature		–65		+150	˚C
Junction Temperature	TJ			+150	˚C
Soldering Temperature				260	˚C

Stresses above listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Driver					
Programmable Driver Output Voltages	VH, VLL, VTT	VEE		VCC	V
DC Driver Output Current	Iout DC	–50		+50	mA
AC Driver Output Current	Iout AC	–180		+180	mA
Output Impedance	Rout	24	30	40	Ω
DUT Pin Capacitance	Cout		10		pF
High Impedance Leakage Current (Note 1)	Ileak		0	4	nA
Comparator					
Input Voltage	VINP	VEE		VCC	V
Input Leakage Current (Note 1)	IBIAS		0	2	nA
Input Capacitance	Cin		4		pF
Offset Voltage	VOS				
@ 0V		10		210	mV
@ 3.0V		–25		175	mV
@ 6.0V		–65		135	mV
@ 7.0V		–78		122	mV
Receiver Threshold	CVA, CVB	VEE + 0.1		VCC – 1.5	V
Threshold Bias Current (Note 1)			0	10	nA
Digital Output High Level (Note 2)	HIGH LEVEL	–2		5	V
Digital Output Low Level (Note 2)	LOW LEVEL	–2		5	V
Analog Switches					
On Resistance					
SW0, SW3	Ron	24	30	37	Ω
SW1, SW2	Ron	75	100	130	Ω
On Resistance - KSW0 - KSW2	Ron	.7	1	1.3	KΩ
High Impedance Leakage Current					
LOAD0 (Note 1)			0	2	nA
LOAD1 (Note 1)			0	2	nA
Power Supply					
Positive Supply Current	ICC		30	45	mA
Negative Supply Current	IEE	–45	–30		mA
Total Leakage (Note 1) (DOUT + VINP + LOAD0 + LOAD1)			0	10	nA

Note 1: This parameter is guaranteed by design and characterization. Production testing is performed against a ± 250 nA limit.

Note 2: –2V or VEE, whichever is more positive.

DC Characteristics *(continued)*

Digital Inputs
DATA, DVR EN*, VTT EN, SW0 EN*, SW1 EN*, SW2 EN*, SW3 EN*

Parameter	Symbol	Min	Typ	Max	Units
Input High Voltage	Input – VBB	500			mV
Input Low Voltage	VCC – Input	500			mV
Input Current	I_{IN}		0	1.0	µA

Digital Outputs
COMPA, COMPB

Parameter	Symbol	Min	Typ	Max	Units
Output Voltage High (Note 1)	VOH	HIGH LEVEL – .3	HIGH LEVEL	HIGH LEVEL + .3	V
Output Voltage Low (Note 2)	VOL	LOW LEVEL – .3	LOW LEVEL	LOW LEVEL + .3	V
DC Output Current	IOUT				mA

Note 1: Output current of –4 µA.
Note 2: Output current of 4 µA.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Driver					
Propagation Delay					
DATA IN to DOUT			18	23	ns
DVR EN* to HiZ			18	23	ns
DVR EN* to VTT			18	23	ns
Minimum Pulse Width (3V Swing)		10			ns
DOUT Output Rise/Fall Times (Note 1)					
1V Swing (20% – 80%)			1.6		ns
3V Swing (10% – 90%)			2.5		ns
5V Swing (10% – 90%)			3.5		ns
Comparator					
Comparator Digital Outputs (Note 2)					
Rise Time (10% – 90%)	tr		2		ns
Fall Time (10% – 90%)	tf		2		ns
VINP to COMPA, COMPB	Tpd		15	20	ns
Minimum Pulse Width		10			ns
Switch Matrix					
SW3 EN* to Switch On			26	36	ns
SW3 EN* to Switch Off			21	31	ns
SW0, 1, 2 EN* to Switch On/Off			20	70	ns

Note 1: Into 18 inches of 50Ω transmission line terminated with 1KΩ and 5 pF with the proper series termination resistor.

Note 2: LOW LEVEL = 0V, HIGH LEVEL = 3.0V

Ordering Information

Part Number	Package
E846ATF	32-pin TQFP (7 mm x 7 mm)
EVM846ATF	Edge846 Evaluation Module

Contact Information

Semtech Corporation
Test and Measurement Division
10021 Willow Creek Rd., San Diego, CA 92131
Phone: (858)695-1808 FAX (858)695-2633

Revision History

Current Revision Date: October 21, 2002
Previous Revision Date: September 27, 2000

Page #	Section Name	Previous Revision	Current Revision
6	Circuit Description		*Add:* Power Supplies Section

Current Revision Date: September 27, 2000
Previous Revision Date: February 3, 2000

Page #	Section Name	Previous Revision	Current Revision
10	AC Characteristics	DATA IN to DOUT: Typ: 10, Max: 20 DVR EN* to HiZ: Typ: 11, Max: 25 DVR EN* to VTT: Typ: 10, Max: 20	DATA IN to DOUT: Typ: 18, Max: 23 DVR EN* to HiZ: Typ: 18, Max: 23 DVR EN* to VTT: Typ: 18, Max: 23
		VINP to COMPA, COMPB: Typ: 10	VINP to COMPA, COMPB: Typ: 15
		SW3 EN* to switch on/off: Max: 100 SW0, 1, 2 EN* to switch on/off: Max 100	SW3 EN* to switch on: Min: 26, Max: 36 SW3 EN* to switch off: Min: 21, Max: 31 SW0, 1, 2, EN* to switch on/off: Min: 20, Max: 70
			Delete: Note 3

Current Revision Date: February 3, 2000
Previous Revision Date: March 8, 1999

Page #	Section Name	Previous Revision	Current Revision
8	DC Characteristics	On Resistance, SW0, SW3: Min. 20Ω	On Resistance, SW0, SW3: Min. 24Ω

Current Revision Date: March 8, 1999
Previous Revision Date: September 29, 1998

Page #	Section Name	Previous Revision	Current Revision
8	DC Characteristics	Comparator Offset Voltage: Min – 100, Max +100	Comparator Offset Voltage: Min 0, Max +200