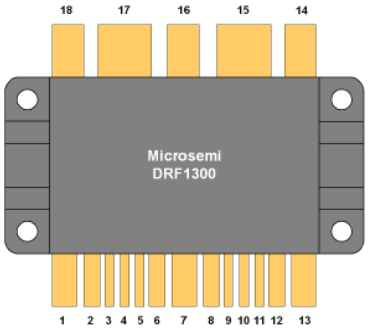
Microsemi
POWER PRODUCTS GROUP

DRF1300
PRELIMINARY

500V, 30A, 30MHz

MOSFET Half Bridge Hybrid

The DRF1300 is a push-pull hybrid containing two high power gate drivers and two power MOSFETs. It was designed to provide the system designer increased flexibility, higher performance, and lowered cost over a non-integrated solution. This low parasitic approach, coupled with the Schmitt trigger input, Kelvin signal ground, Anti-Ring function Invert and Non-invert select pin provide improved stability and control in Kilowatt to Multi-Kilowatt, High Frequency ISM applications.



DRIVER FEATURES

- **Switching Frequency: DC TO 30MHz**
- **Inverting Non-Inverting Select**
- **Low Pulse Width Distortion**
- **Single Power Supply (Per Section)**
- **1VCMOS Schmitt Trigger Input 1V Hysteresis**
- **Drives > 3nF**

MOSFET FEATURES

- **Switching Frequency: DC TO 30MHz**
- **Switching Speed 3-4ns**
- **B_{Vds} = 500V**
- **I_{ds} = 30A avg. Per-section**
- **$R_{ds(on)}$ ≤ .24 Ohm**
- **P_D = 550W Per-section**

TYPICAL APPLICATIONS

- **Class C, D and E RF Generators**
- **Switch Mode Power Amplifiers**
- **HV Pulse Generators**
- **Ultrasound Transducer Drivers**
- **Acoustic Optical Modulators**
- **RoHS Compliant**

Driver Absolute Maximum Ratings (per-Section)

Symbol	Parameter	Ratings	Unit
V_{DD}	Supply Voltage	18	V
V_{IN}	Input Single Voltage	-.7 to +5.5	
$I_{O\,PK}$	Output Current Peak	12	A
T_J	Operating and Storage Temperature	-55 to +175	°C

Driver Specifications (Per-Section)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	8	15	18	V
V_{IN}	Input Voltage	3		5.5	
$V_{IN(R)}$	Input Voltage Rising Edge[6]		3		ns
$V_{IN(F)}$	Input Voltage Falling Edge[6]		3		
I_{DDQ}	Quiescent Current		2		mA
I_O	Output Current		8		A
C_{oss}	Output Capacitance		2500		pF
C_{iss}	Input Capacitance		3		
$V_{T(ON)}$	Input, Low to High Out	0.8		1.1	V
$V_{T(OFF)}$	Input, High to Low Out	1.9		2.2	
T_{DLY}	Time Delay (throughput)		38		ns
ΔT_{DLY}	Delta Time Delay Section A to B	0	0.5	1.5	
t_r	Rise Time[2,3]		5		ns
t_f	Fall Time[2,3]		5		
T_D	Prop. Delay[2,4]		35		

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MOSFET Absolute Maximum Ratings (Per-Section) DRF1300

Symbol	Parameter	Min	Typ	Max	Unit
V_{DSS}	Drain Source Voltage		500		V
I_D	Continuous Drain Current T_{HS} = 25°C		30		A
$R_{DS(on)}$	Drain-Source On State Resistance		0.24		Ω

Dynamic Characteristics (Per-Section)

Symbol	Parameter	Min	Typ	Max	Unit
C_{iss}	Input Capacitance		1800	2000	pF
C_{oss}	Output Capacitance		335	400	
C_{rss}	Reverse Transfer Capacitance		75	80	

Thermal Characteristics (Total Package)

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Junction to Case Thermal Resistance	.06	°C/W
$R_{\theta JHS}$	Junction to Heat Sink Thermal Resistance	.134	
T_{JSTG}	Storage Junction Temperature	-55 to 150	°C
P_D	Maximum Power Dissipation @ T_{SINK} = 25°C	1.1	KW
P_{DC}	Total Power Dissipation @ T_C = 25°C	2.5	

Section A and B Output Switching Performance

Symbol	Characteristic	Min	Typ	Max	Typ
T_{ON}	Leading Edge 10% to 90%	2	3	4	ns
T_{OFF}	Trailing Edge 10% to 90%, See Note 1	45	TBD	49	
$T_{DLY(ON)}$	Total Throughput Delay Time, ON	47	TBD	45	
$T_{DLY(OFF)}$	Total Throughput Delay Time, OFF, See Note 1	49	50	51	
$\Delta T_{DLY(ON)}$	Delta T_{ON} Delay between Section A and B	-0.5	0	1.5	
$\Delta T_{DLY(OFF)}$	Delta T_{OFF} Delay between Section A and B, See Note 1	0	0.6	1.3	

NOTE: This parameter is Test Fixture Dependant, See Test Fixture R_L = 50Ω RC time constant C_{OSS} and R_L Test circuit shown in figure 2. All measurements were made with the Anti-Ring circuit activated unless noted

1. Symmetry is the percent difference in high and low FWHM times with a 50% duty cycle square wave input.
2. R_L = 50Ω, C_L = 3000pF
3. 10% - 90%, see Test Circuit
4. 50% - 50%, see Test Circuit

Microsemi reserves the right to change, without notice, the specifications and information contained herein.

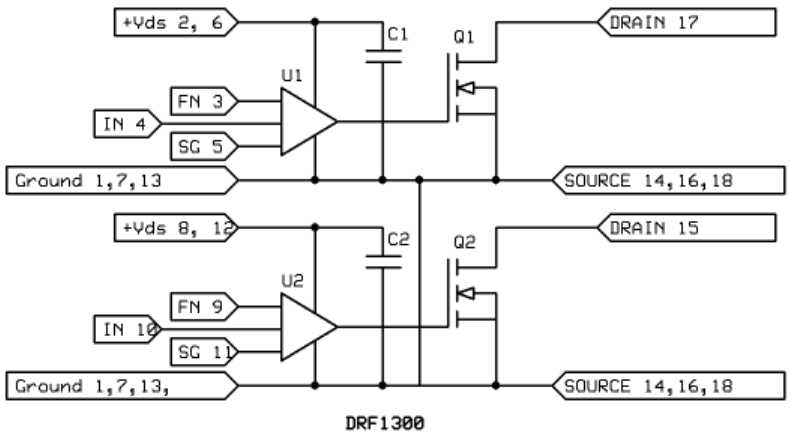

Figure 1, DRF1300 Test Circuit Diagram

The DRF1300 is a Push-Pull hybrid, see Figure 1, the device incorporates two MOSFET drivers and two power MOSFETs. The drivers are designed to apply up to 18 Volts of gate drive with sufficient current capability to charge the gates of any of the RF MOSFETs at PPG Commercial RF. The specifications for the driver are listed on the first page of this data sheet. For an in depth discussion of the driver IC performance, see the DRF100FL data sheet. The driver incorporates an anti-ring function, an invert non-invert pin. The input control signal has an accompanying signal ground pin the pair for a Kelvin connection for improved noise immunity. The hybrid also includes high speed bypass capacitors for the driver. This provides high speed gate drive for fast switching. Typical switching speed for the MOSFET is in the range of 3 to 4ns. The two sections of the DRF1300 are completely independent. To further increase the utility of the device, the driver die and the MOSFET die are adjacent die selected. This provides a very close match in the turn-on and the propagation delays.

None of the inputs to U1 or U2 of the DRF1300 are isolated for direct connection to a ground referenced power supply or control circuitry. **Isolation appropriate to a half or full bridge configuration is the responsibility of the end user.** The IN pin is the input for the control signal and is applied to a Schmitt Trigger. The SG pin, a Kelvin return, is reserved for the control signal ground return only.

The Function (FN, pin 3) is the invert or non-invert select Pin, it is Internally held high, Normally Non-inverting.

Truth Table			
FN (pin 3)	**IN (pin 4)**	**MOSFET**	**Function**
HIGH	**HIGH**	**ON**	**Non-Invert**
HIGH	**LOW**	**OFF**	**Non-Invert**
LOW	**HIGH**	**OFF**	**Inverting**
LOW	**LOW**	**ON**	**Inverting**

On the output side are the Drain (17), Source (15) Output (16) and the C3 Bypass (18, 19) connections. It is imperative that output currents be restricted to these pins by design. See DRF100 for more information on Driver CI used in the device.

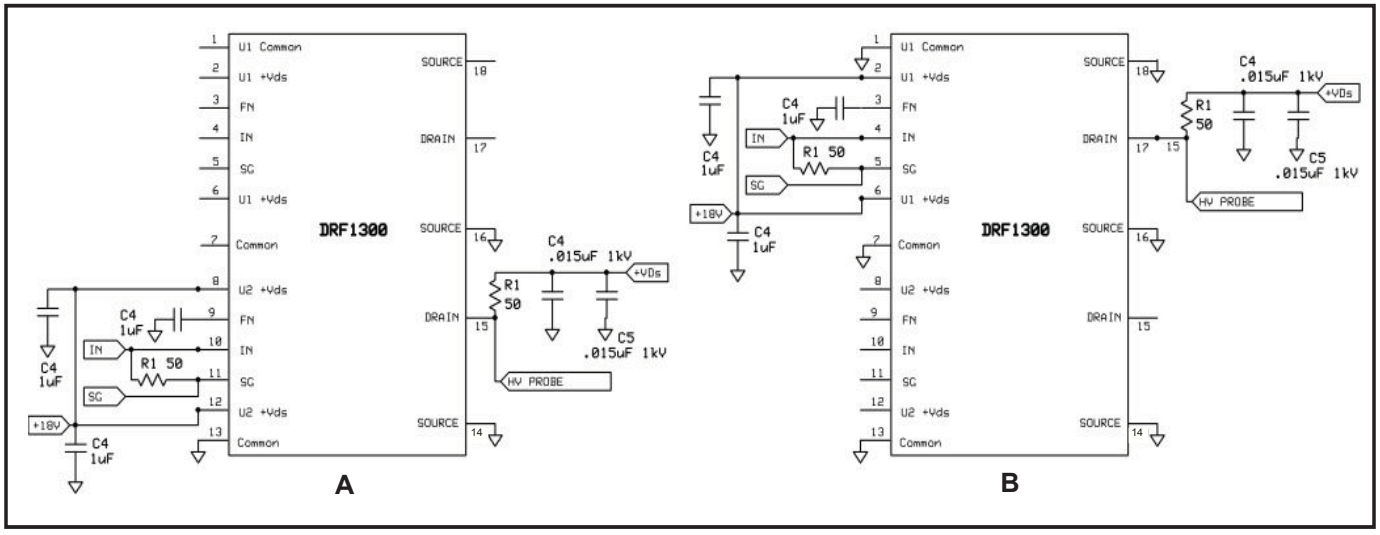

Figure 2, DRF1300 Test Circuit

The DRF1300 test circuit is illustrated in Figure 2. Each side of the hybrid is tested independently. The FN pin is by-passed with a 1uF capacitor, C4, to insure noise immunity. The input control signal with the Kelvin ground is applied to the IN and SG pins. The +Vdd power is applied to both Pin 8 and Pin 12 for lower device and pin 6 and pin 2 for the upper device. These pins should be heavily bypassed, the parallel combination of a .47uF chip and a 10uF chip is recommended. These capacitors should be placed as close to the pins as possible. All switching and frequency data was acquired with this circuit.

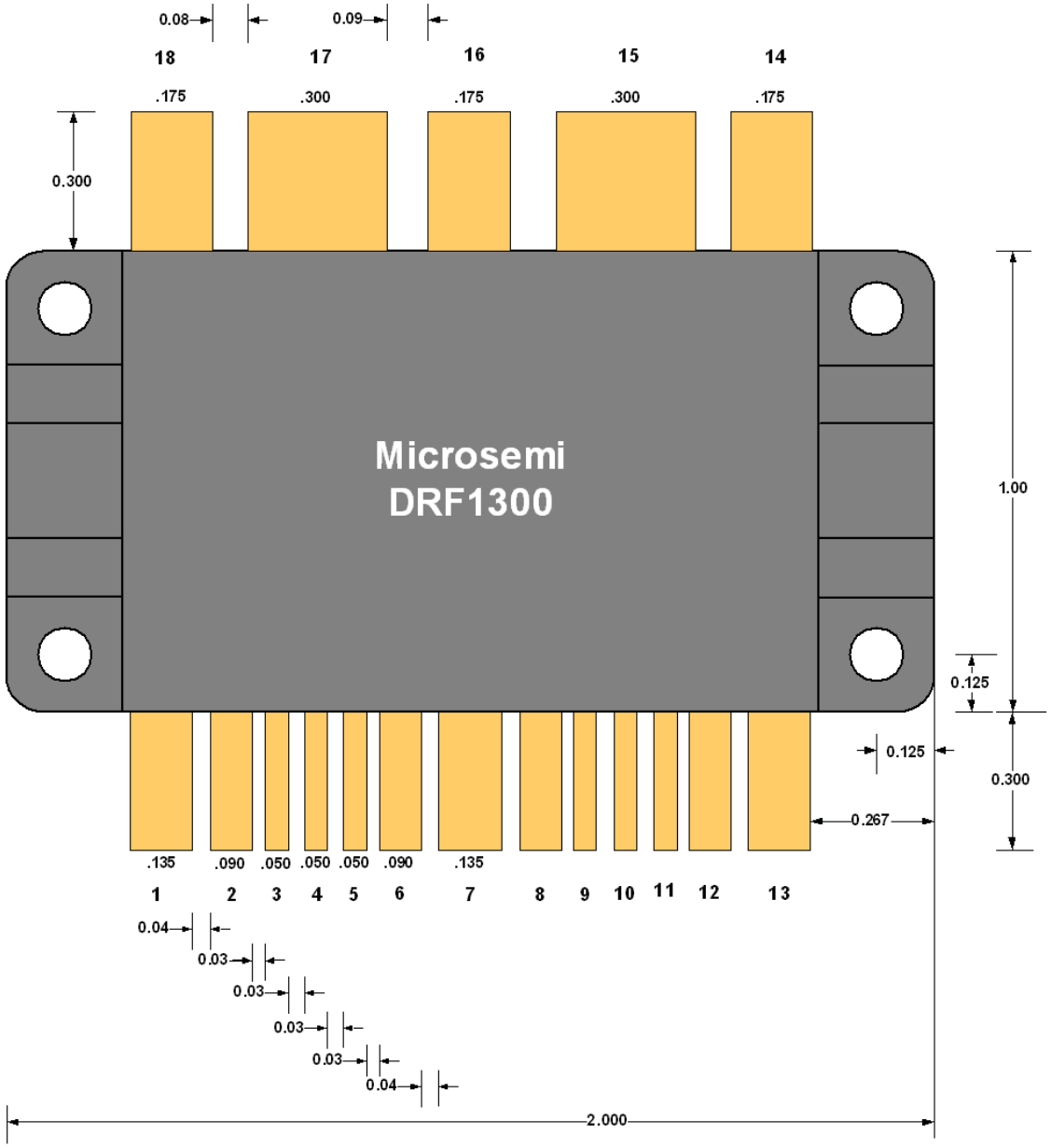

Figure 4, DRF1300 Mechanical Outline
All dimensions are ± .005

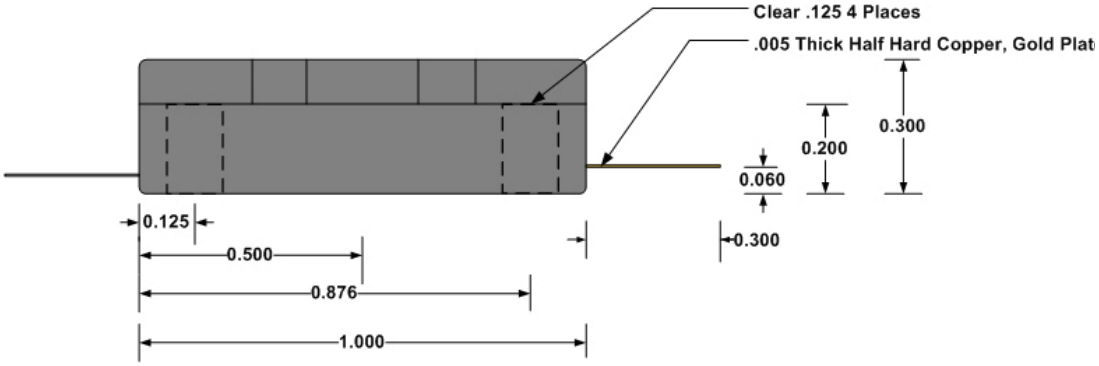

Figure 5, DRF1300 Side View Outline