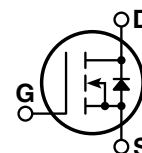
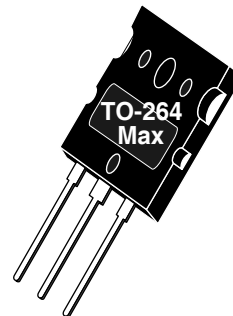


POWER MOS V® FREDFET

Power MOS V® is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimizes the JFET effect, increases packing density and reduces the on-resistance. Power MOS V® also achieves faster switching speeds through optimized gate layout.



- TO-264 MAX Package
- Avalanche Energy Rated
- Faster Switching
- **FAST RECOVERY BODY DIODE**
- Lower Leakage

MAXIMUM RATINGS

All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT10030L2VFR	UNIT
V_{DSS}	Drain-Source Voltage	1000	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	33	Amps
I_{DM}	Pulsed Drain Current ^①	132	
V_{GS}	Gate-Source Voltage Continuous	± 30	Volts
V_{GSM}	Gate-Source Voltage Transient	± 40	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	833	Watts
	Linear Derating Factor	6.66	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ^① (Repetitive and Non-Repetitive)	33	Amps
E_{AR}	Repetitive Avalanche Energy ^①	50	mJ
E_{AS}	Single Pulse Avalanche Energy ^④	3200	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu A$)	1000			Volts
$R_{DS(on)}$	Drain-Source On-State Resistance ^② ($V_{GS} = 10V, I_D = 16.5A$)			0.300	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = 1000V, V_{GS} = 0V$)			250	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 800V, V_{GS} = 0V, T_C = 125^\circ\text{C}$)			1000	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 5mA$)	2		4	Volts

 **CAUTION:** These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

DYNAMIC CHARACTERISTICS

APT10030L2VFR

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C_{iss}	Input Capacitance	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1\text{ MHz}$		10600		pF
C_{oss}	Output Capacitance			1000		
C_{rss}	Reverse Transfer Capacitance			500		
Q_g	Total Gate Charge ③	$V_{GS} = 10V$ $V_{DD} = 500V$ $I_D = 33A @ 25^\circ C$		585		nC
Q_{gs}	Gate-Source Charge			55		
Q_{gd}	Gate-Drain ("Miller") Charge			265		
$t_{d(on)}$	Turn-on Delay Time	$V_{GS} = 15V$ $V_{DD} = 500V$ $I_D = 33A @ 25^\circ C$ $R_G = 0.6\Omega$		14		ns
t_r	Rise Time			16		
$t_{d(off)}$	Turn-off Delay Time			75		
t_f	Fall Time			14		

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I_S	Continuous Source Current (Body Diode)			33	Amps
I_{SM}	Pulsed Source Current ① (Body Diode)			132	
V_{SD}	Diode Forward Voltage ② ($V_{GS} = 0V$, $I_S = -33A$)			1.3	Volts
dv/dt	Peak Diode Recovery dv/dt ⑤			18	V/ns
t_{rr}	Reverse Recovery Time ($I_S = -33A$, $di/dt = 100A/\mu s$)	$T_j = 25^\circ C$		310	ns
		$T_j = 125^\circ C$		625	
Q_{rr}	Reverse Recovery Charge ($I_S = -33A$, $di/dt = 100A/\mu s$)	$T_j = 25^\circ C$	2.0		μC
		$T_j = 125^\circ C$	6.0		
I_{RRM}	Peak Recovery Current ($I_S = -33A$, $di/dt = 100A/\mu s$)	$T_j = 25^\circ C$	15		Amps
		$T_j = 125^\circ C$	26		

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.15	$^\circ C/W$
$R_{\theta JA}$	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature

② Pulse Test: Pulse width < 380 μs , Duty Cycle < 2%

③ See MIL-STD-750 Method 3471

④ Starting $T_j = +25^\circ C$, $L = 5.88mH$, $R_G = 25\Omega$, Peak $I_L = 33A$

⑤ dv/dt numbers reflect the limitations of the test circuit rather than the device itself. $I_S \leq -I_D 33A$ $di/dt \leq 700A/\mu s$ $v_R \leq 1000V$ $T_j \leq 150^\circ C$

APT Reserves the right to change, without notice, the specifications and information contained herein.

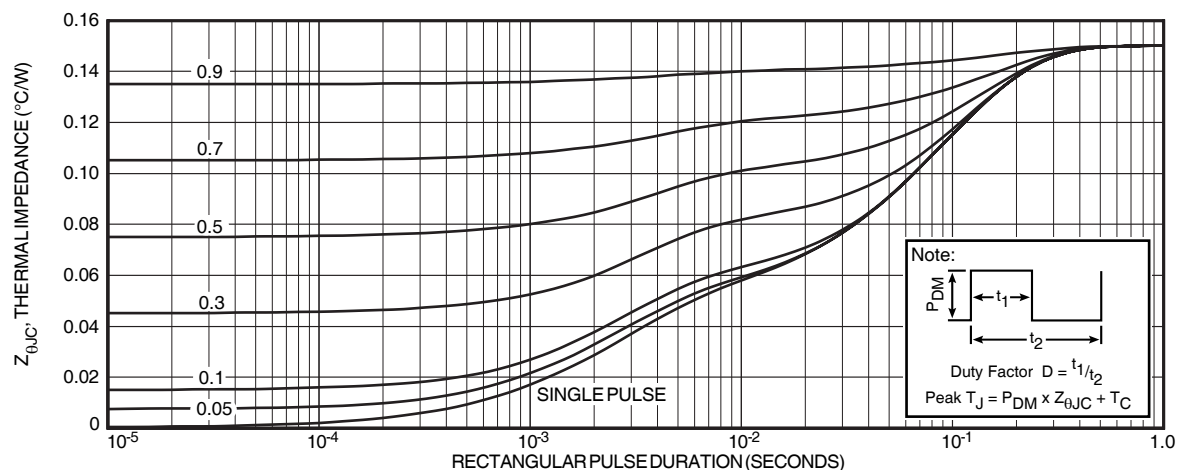


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Typical Performance Curves

APT10030L2VFR

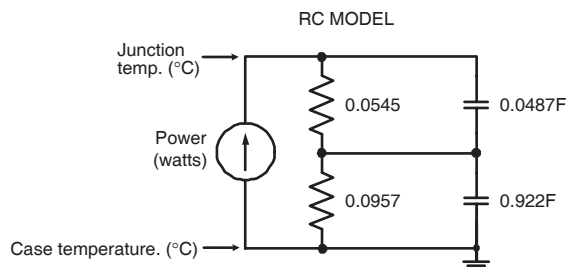


FIGURE 2, TRANSIENT THERMAL IMPEDANCE MODEL

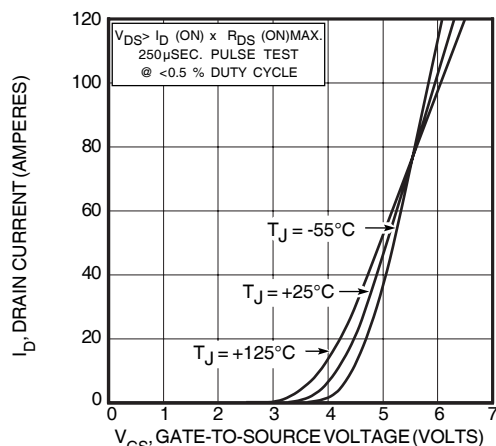


FIGURE 4, TRANSFER CHARACTERISTICS

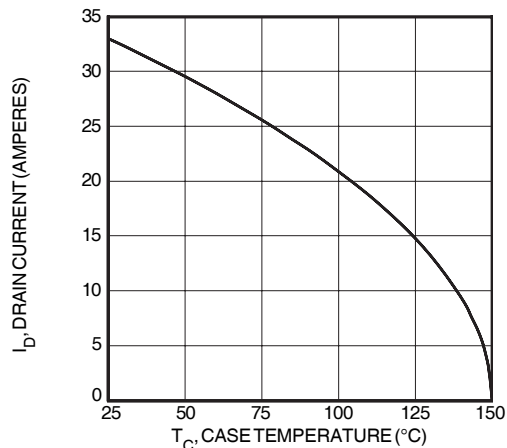


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

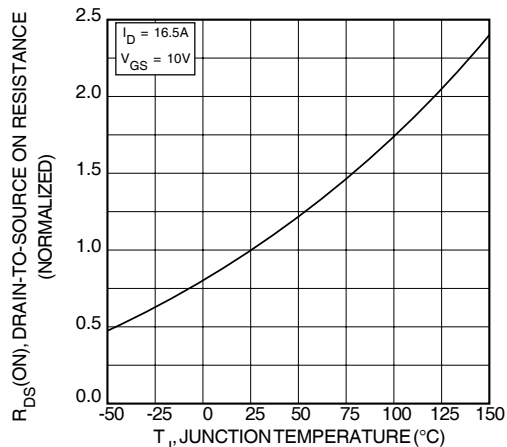


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

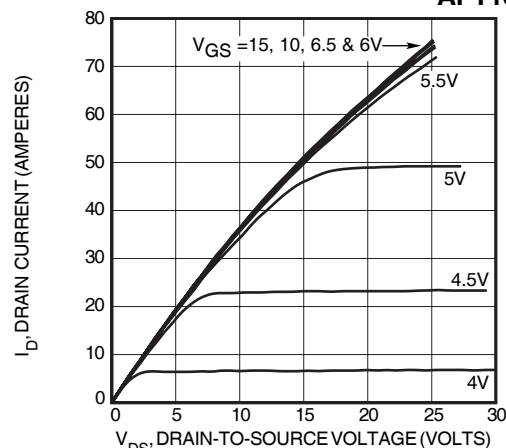


FIGURE 3, LOW VOLTAGE OUTPUT CHARACTERISTICS

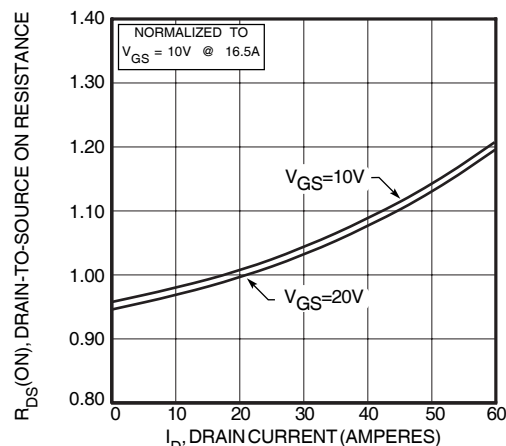


FIGURE 5, $R_{DS}(ON)$ vs DRAIN CURRENT

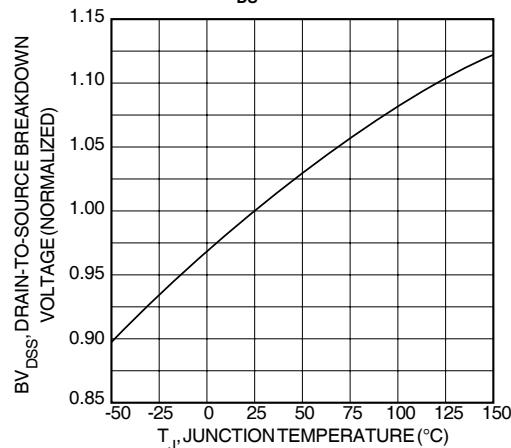


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

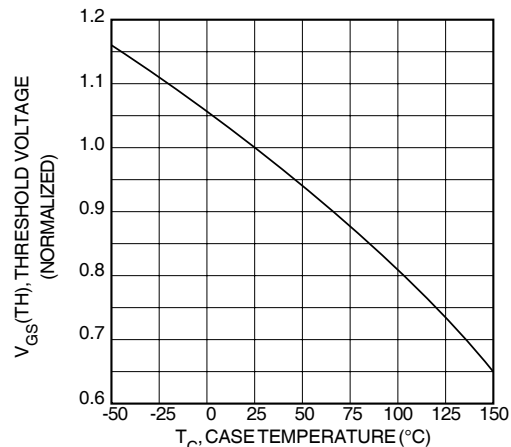


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

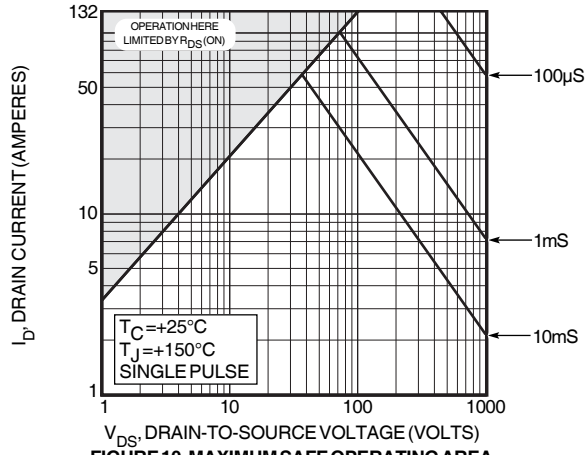


FIGURE 10, MAXIMUM SAFE OPERATING AREA

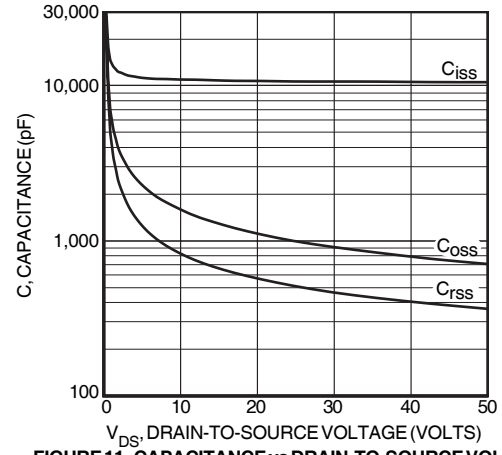


FIGURE 11, CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

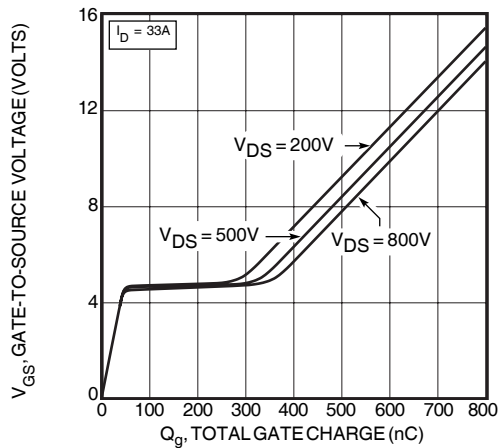


FIGURE 12, GATE CHARGES vs GATE-TO-SOURCE VOLTAGE

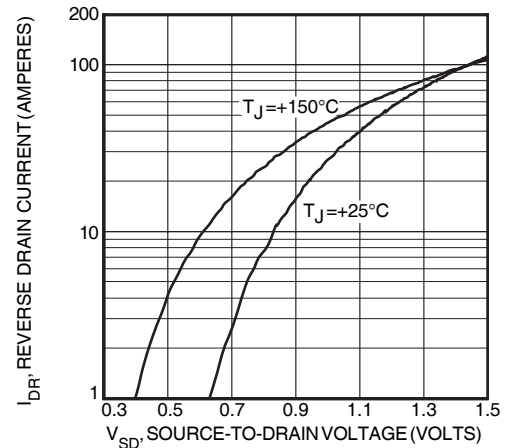


FIGURE 13, SOURCE-DRAIN DIODE FORWARD VOLTAGE

TO-264 MAX™(L2) Package Outline

