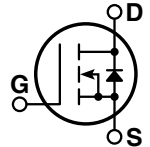
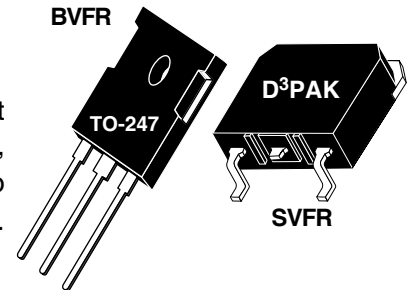


POWER MOS V®

FREDFET

Power MOS V® is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimizes the JFET effect, increases packing density and reduces the on-resistance. Power MOS V® also achieves faster switching speeds through optimized gate layout.



- Lower Leakage
- 100% Avalanche Tested
- Faster Switching
- Fast Recovery Body Diode
- TO-247 or Surface Mount D³PAK Package

MAXIMUM RATINGS

All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT20M38BVFR_SVFR	UNIT
V_{DSS}	Drain-Source Voltage	200	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	67	Amps
I_{DM}	Pulsed Drain Current ^①	268	
V_{GS}	Gate-Source Voltage Continuous	± 30	Volts
V_{GSM}	Gate-Source Voltage Transient	± 40	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	370	Watts
	Linear Derating Factor	2.96	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ^① (Repetitive and Non-Repetitive)	67	Amps
E_{AR}	Repetitive Avalanche Energy ^①	30	mJ
E_{AS}	Single Pulse Avalanche Energy ^④	1300	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu A$)	200			Volts
$I_{D(on)}$	On State Drain Current ^② ($V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max, $V_{GS} = 10V$)	67			Amps
$R_{DS(on)}$	Drain-Source On-State Resistance ^② ($V_{GS} = 10V, 0.5 I_{D[Cont.]}$)			0.038	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = V_{DSS}, V_{GS} = 0V$)			250	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 0.8 V_{DSS}, V_{GS} = 0V, T_C = 125^\circ\text{C}$)			1000	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1.0mA$)	2		4	Volts



CAUTION: These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

APT Website - <http://www.advancedpower.com>

DYNAMIC CHARACTERISTICS

APT20M38BVFR_SVFR

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C_{iss}	Input Capacitance	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1 \text{ MHz}$		5100	6120	pF
C_{oss}	Output Capacitance			1145	1600	
C_{rss}	Reverse Transfer Capacitance			390	585	
Q_g	Total Gate Charge ^③	$V_{GS} = 10V$ $V_{DD} = 0.5 V_{DSS}$ $I_D = I_D [\text{Cont.}] @ 25^\circ\text{C}$		148	225	nC
Q_{gs}	Gate-Source Charge			47	75	
Q_{gd}	Gate-Drain ("Miller") Charge			75	110	
$t_{d(on)}$	Turn-on Delay Time	$V_{GS} = 15V$ $V_{DD} = 0.5 V_{DSS}$ $I_D = I_D [\text{Cont.}] @ 25^\circ\text{C}$ $R_G = 1.6\Omega$		14	28	ns
t_r	Rise Time			21	42	
$t_{d(off)}$	Turn-off Delay Time			48	75	
t_f	Fall Time			10	20	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I_S	Continuous Source Current (Body Diode)			67	Amps
I_{SM}	Pulsed Source Current ^① (Body Diode)			268	
V_{SD}	Diode Forward Voltage ^② ($V_{GS} = 0V$, $I_S = -I_D [\text{Cont.}]$)			1.3	Volts
dv/dt	Peak Diode Recovery dv/dt ^⑤			8	V/ns
t_{rr}	Reverse Recovery Time ($I_S = -I_D [\text{Cont.}]$, $di/dt = 100A/\mu s$)	$T_j = 25^\circ\text{C}$		240	ns
		$T_j = 125^\circ\text{C}$		420	
Q_{rr}	Reverse Recovery Charge ($I_S = -I_D [\text{Cont.}]$, $di/dt = 100A/\mu s$)	$T_j = 25^\circ\text{C}$	1		μC
		$T_j = 125^\circ\text{C}$	2		
I_{RRM}	Peak Recovery Current ($I_S = -I_D [\text{Cont.}]$, $di/dt = 100A/\mu s$)	$T_j = 25^\circ\text{C}$	10		Amps
		$T_j = 125^\circ\text{C}$	16		

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.34	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature.

② Pulse Test: Pulse width < 380 μs , Duty Cycle < 2%

③ See MIL-STD-750 Method 3471

④ Starting $T_j = +25^\circ\text{C}$, $L = 0.58\text{mH}$, $R_G = 25\Omega$, Peak $I_L = 67A$

⑤ $I_S = -I_D [\text{Cont.}]$, $di/dt = 100A/\mu s$, $V_{DD} = V_{DSS}$, $T_j = 150^\circ\text{C}$, $R_G = 2.0\Omega$, $V_R = 200V$.

APT Reserves the right to change, without notice, the specifications and information contained herein.

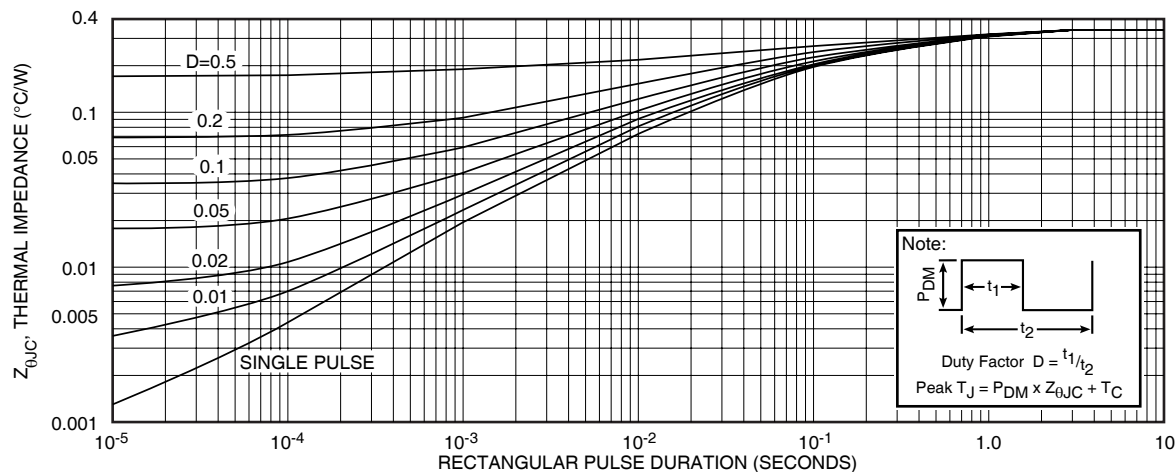


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

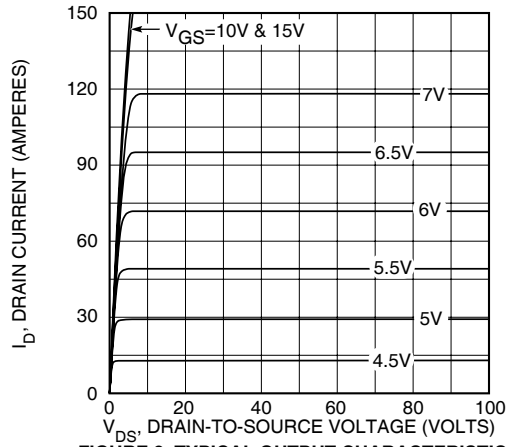


FIGURE 2, TYPICAL OUTPUT CHARACTERISTICS

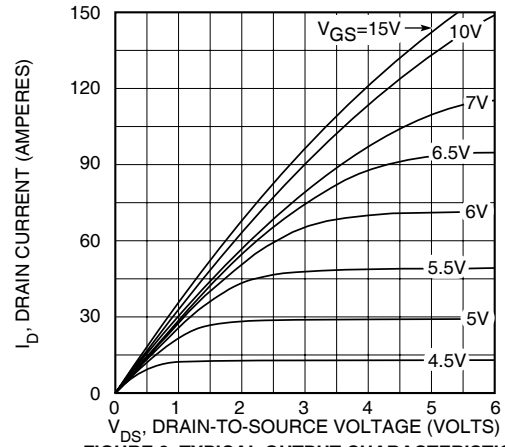


FIGURE 3, TYPICAL OUTPUT CHARACTERISTICS

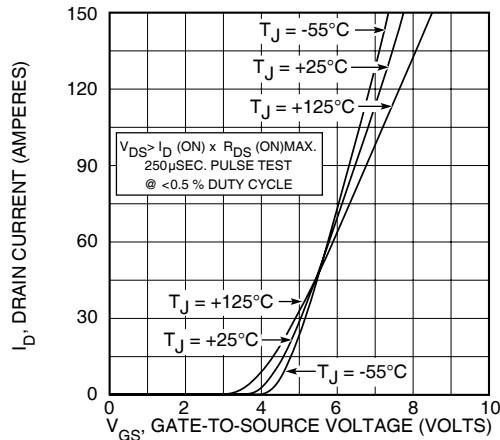


FIGURE 4, TYPICAL TRANSFER CHARACTERISTICS

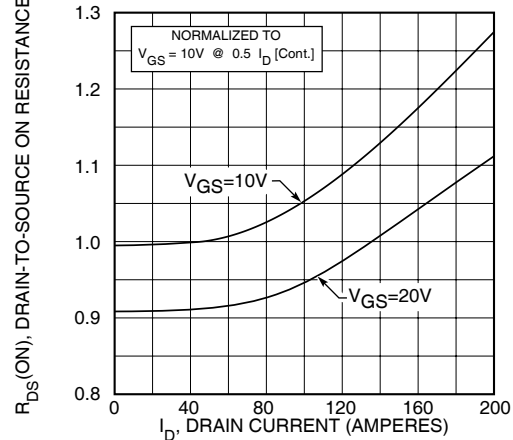


FIGURE 5, $R_{DS(ON)}$ vs DRAIN CURRENT

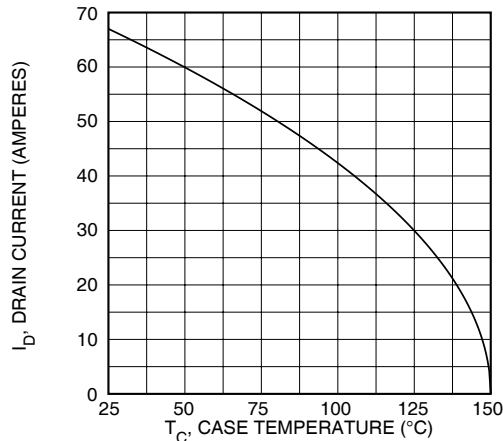


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

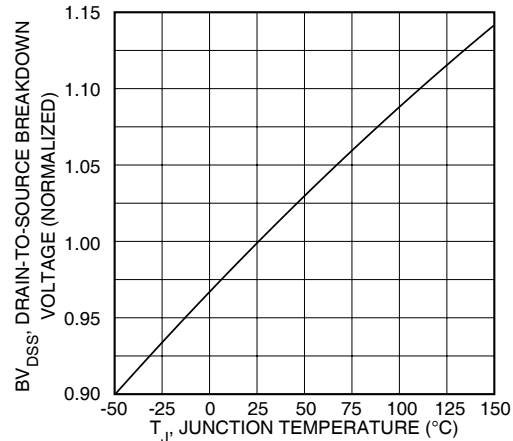


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

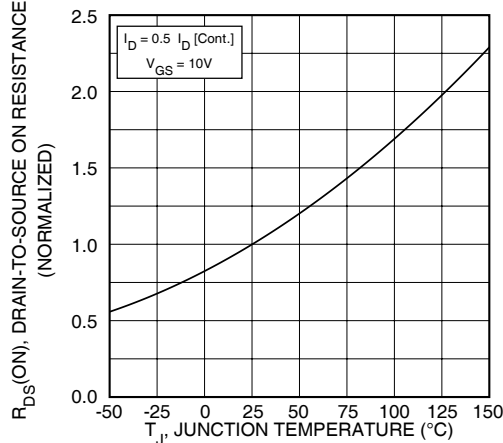


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

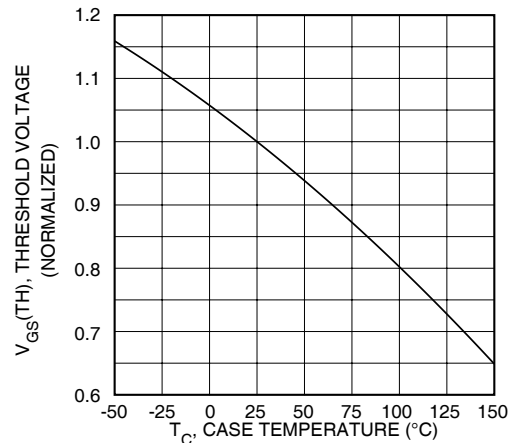


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

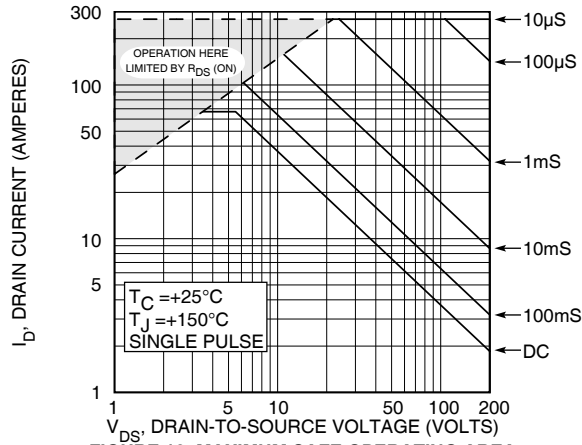


FIGURE 10, MAXIMUM SAFE OPERATING AREA

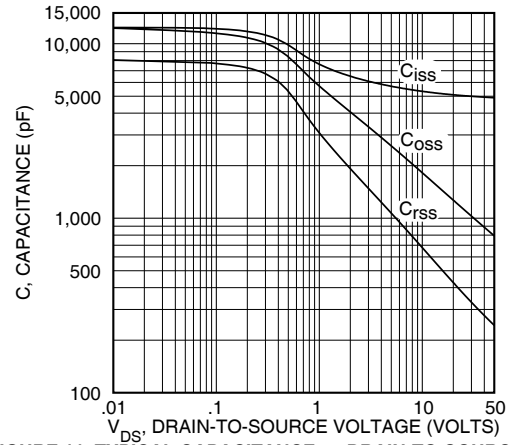


FIGURE 11, TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

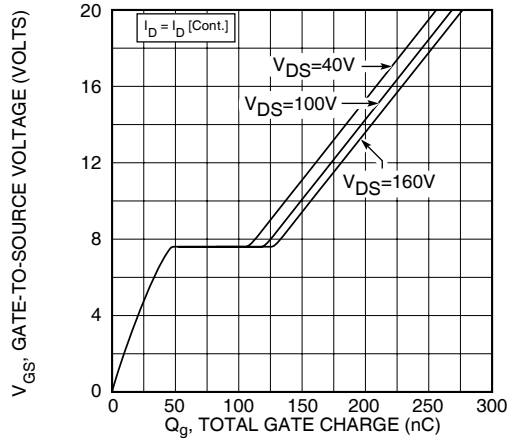


FIGURE 12, GATE CHARGES vs GATE-TO-SOURCE VOLTAGE

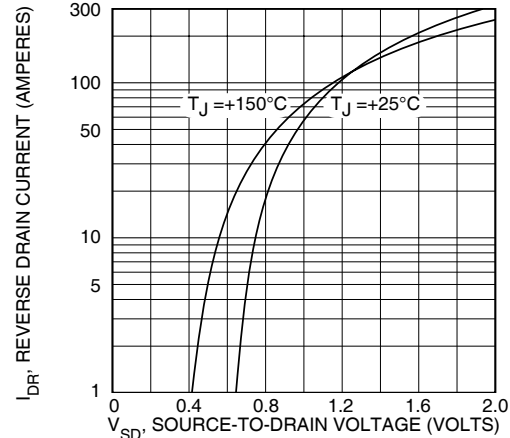
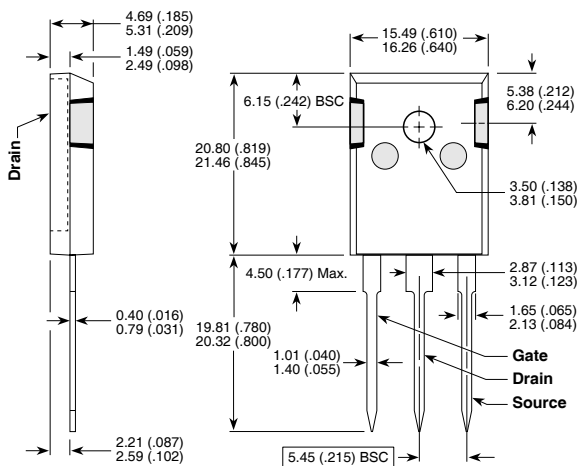


FIGURE 13, TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

TO-247 Package Outline (BVFR)

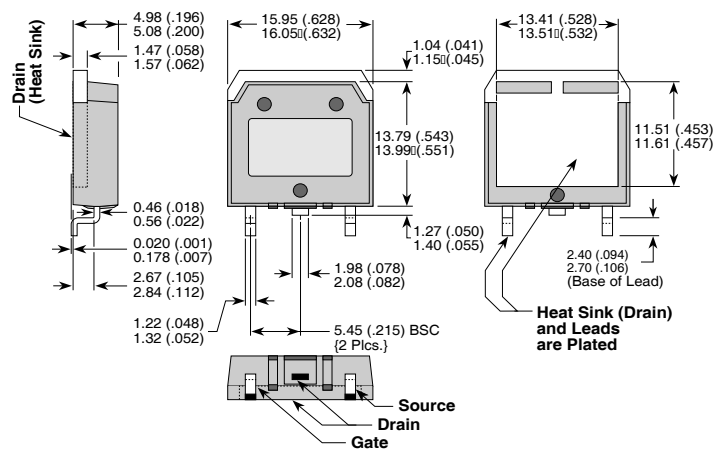


Dimensions in Millimeters and (Inches)

APT's products are covered by one or more of U.S. patents 4,895,810 5,045,903 5,089,434 5,182,234 5,019,522

5,262,336 6,503,786 5,256,583 4,748,103 5,283,202 5,231,474 5,434,095 5,528,058 and foreign patents. US and Foreign patents pending. All Rights Reserved.

D³PAK Package Outline (SVFR)



Dimensions in Millimeters (Inches)