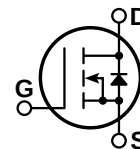


POWER MOS 7® FREDFET

Power MOS 7® is a new generation of low loss, high voltage, N-Channel enhancement mode power MOSFETS. Both conduction and switching losses are addressed with Power MOS 7® by significantly lowering $R_{DS(ON)}$ and Q_g . Power MOS 7® combines lower conduction and switching losses along with exceptionally fast switching speeds inherent with APT's patented metal gate structure.



- Lower Input Capacitance
- Lower Miller Capacitance
- Lower Gate Charge, Q_g
- Increased Power Dissipation
- Easier To Drive
- Popular SOT-227 Package
- **FAST RECOVERY BODY DIODE**



MAXIMUM RATINGS

All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT12031JLL	UNIT
V_{DSS}	Drain-Source Voltage	1200	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	30	Amps
I_{DM}	Pulsed Drain Current ^①	120	
V_{GS}	Gate-Source Voltage Continuous	± 30	Volts
V_{GSM}	Gate-Source Voltage Transient	± 40	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	690	Watts
	Linear Derating Factor	5.52	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ^① (Repetitive and Non-Repetitive)	30	Amps
E_{AR}	Repetitive Avalanche Energy ^①	50	mJ
E_{AS}	Single Pulse Avalanche Energy ^④	3600	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu A$)	1200			Volts
$R_{DS(on)}$	Drain-Source On-State Resistance ^② ($V_{GS} = 10V, 15A$)			0.310	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = 1200V, V_{GS} = 0V$)			250	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 960V, V_{GS} = 0V, T_C = 125^\circ\text{C}$)			1000	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 5mA$)	3		5	Volts

 **CAUTION:** These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

APT Website - <http://www.advancedpower.com>

DYNAMIC CHARACTERISTICS

APT12031JFLL

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C_{iss}	Input Capacitance	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1\text{ MHz}$		9480		pF
C_{oss}	Output Capacitance			1460		
C_{rss}	Reverse Transfer Capacitance			250		
Q_g	Total Gate Charge ③	$V_{GS} = 10V$ $V_{DD} = 600V$ $I_D = 30A @ 25^\circ C$		365		nC
Q_{gs}	Gate-Source Charge			45		
Q_{gd}	Gate-Drain ("Miller") Charge			235		
$t_{d(on)}$	Turn-on Delay Time	RESISTIVE SWITCHING $V_{GS} = 15V$ $V_{DD} = 600V$ $I_D = 30A @ 25^\circ C$ $R_G = 0.6\Omega$		23		ns
t_r	Rise Time			16		
$t_{d(off)}$	Turn-off Delay Time			79		
t_f	Fall Time			30		
E_{on}	Turn-on Switching Energy ⑥	INDUCTIVE SWITCHING @ 25°C $V_{DD} = 800V, V_{GS} = 15V$ $I_D = 30A, R_G = 5\Omega$		1760		μJ
E_{off}	Turn-off Switching Energy			1241		
E_{on}	Turn-on Switching Energy ⑥	INDUCTIVE SWITCHING @ 125°C $V_{DD} = 800V, V_{GS} = 15V$ $I_D = 30A, R_G = 5\Omega$		3035		
E_{off}	Turn-off Switching Energy			1557		

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I_S	Continuous Source Current (Body Diode)			30	Amps
I_{SM}	Pulsed Source Current ① (Body Diode)			120	
V_{SD}	Diode Forward Voltage ② ($V_{GS} = 0V, I_S = -30A$)			1.3	Volts
dv/dt	Peak Diode Recovery dv/dt ⑤			18	V/ns
t_{rr}	Reverse Recovery Time ($I_S = -30A, di/dt = 100A/\mu s$)	$T_j = 25^\circ C$		300	ns
		$T_j = 125^\circ C$		600	
Q_{rr}	Reverse Recovery Charge ($I_S = -30A, di/dt = 100A/\mu s$)	$T_j = 25^\circ C$	1.8		μC
		$T_j = 125^\circ C$	7.4		
I_{RRM}	Peak Recovery Current ($I_S = -30A, di/dt = 100A/\mu s$)	$T_j = 25^\circ C$	16		Amps
		$T_j = 125^\circ C$	30		

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.18	$^\circ C/W$
$R_{\theta JA}$	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature

② Pulse Test: Pulse width < 380 μs , Duty Cycle < 2%

③ See MIL-STD-750 Method 3471

④ Starting $T_j = +25^\circ C$, $L = 8.0mH$, $R_G = 25\Omega$, Peak $I_L = 30A$

⑤ dv/dt numbers reflect the limitations of the test circuit rather than the device itself. $I_S \leq -I_{D30A}$ $di/dt \leq 700A/\mu s$ $V_R \leq V_{DSS}$ $T_j \leq 150^\circ C$

⑥ E_{on} includes diode reverse recovery. See figures 18, 20.

APT Reserves the right to change, without notice, the specifications and information contained herein.

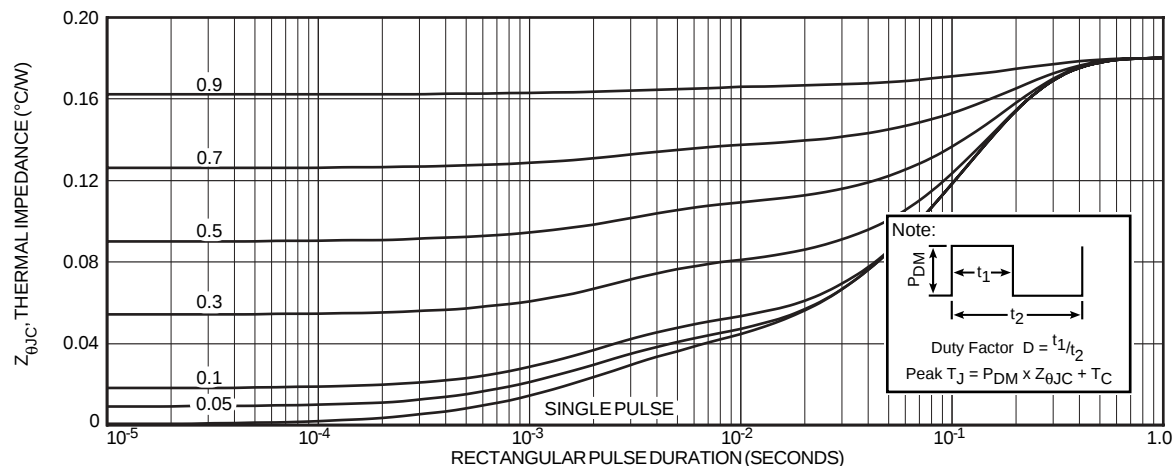


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Typical Performance Curves

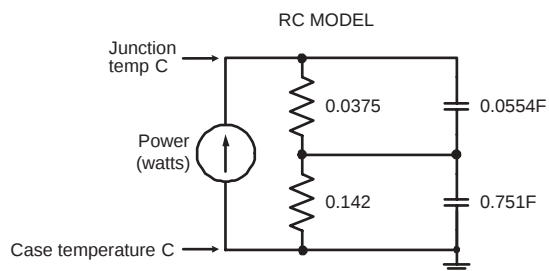


FIGURE2, TRANSIENT THERMAL IMPEDANCE MODEL

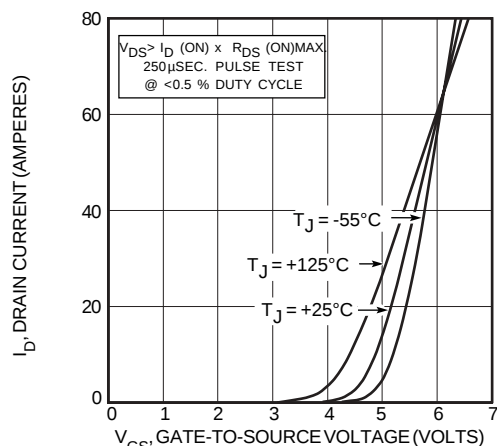


FIGURE4, TRANSFER CHARACTERISTICS

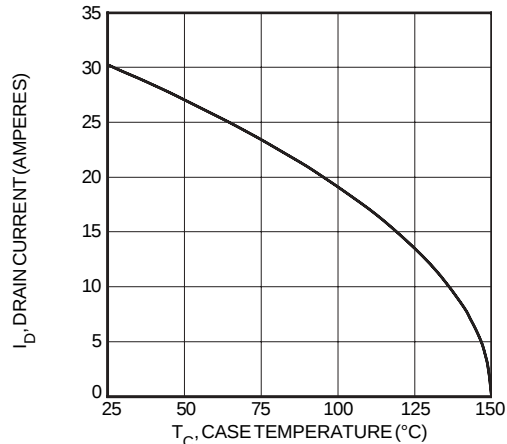


FIGURE6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

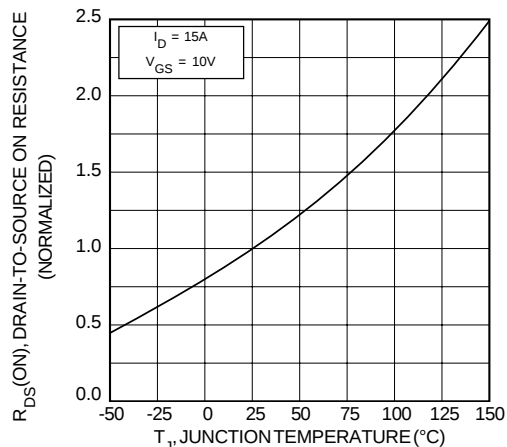


FIGURE8, ON-RESISTANCE vs. TEMPERATURE

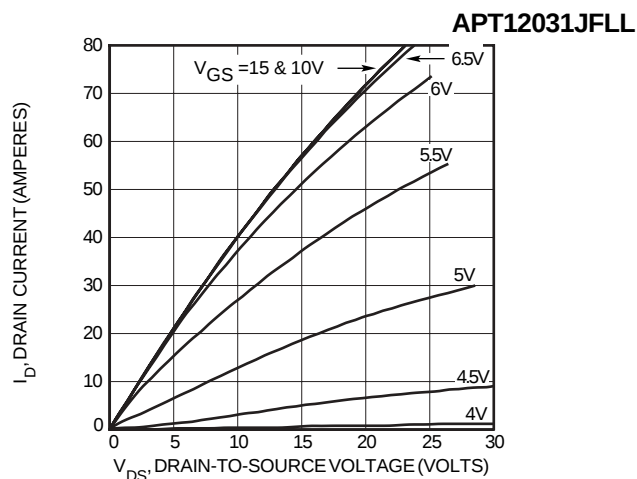


FIGURE3, LOW VOLTAGE OUTPUT CHARACTERISTICS

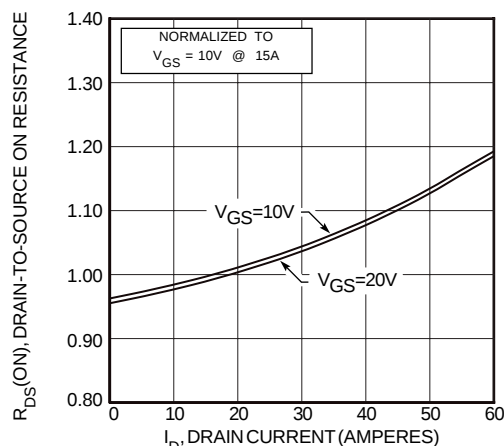


FIGURE5, $R_{DS(ON)}$ vs DRAIN CURRENT

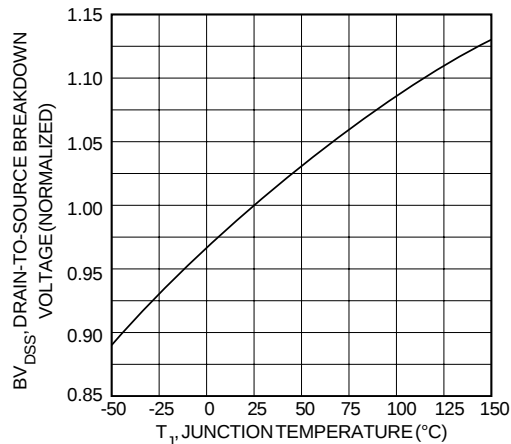


FIGURE7, BREAKDOWN VOLTAGE vs TEMPERATURE

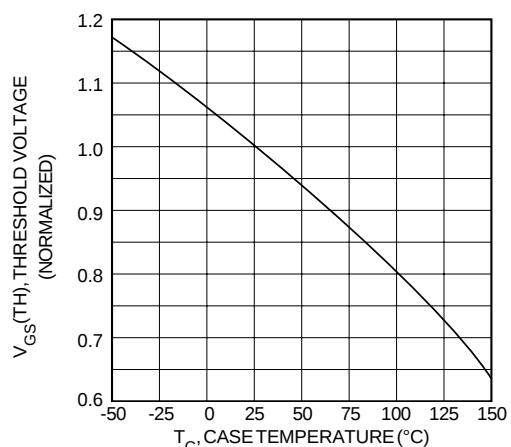


FIGURE9, THRESHOLD VOLTAGE vs TEMPERATURE

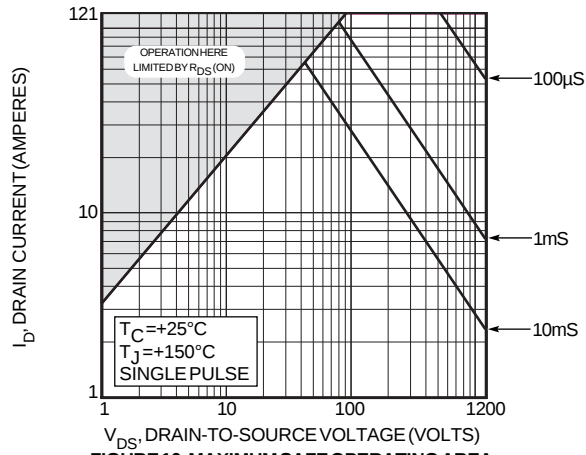


FIGURE 10, MAXIMUM SAFE OPERATING AREA

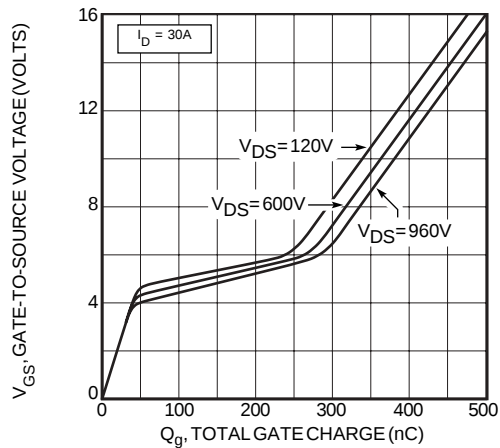


FIGURE 12, GATE CHARGES vs GATE-TO-SOURCE VOLTAGE

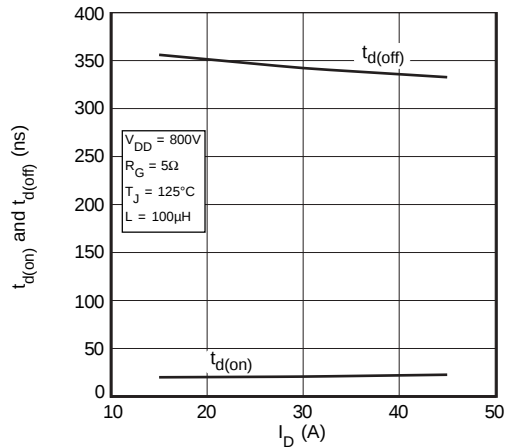


FIGURE 14, DELAY TIMES vs CURRENT

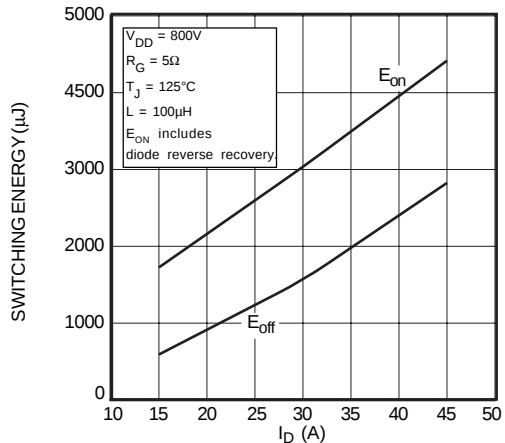


FIGURE 16, SWITCHING ENERGY vs CURRENT

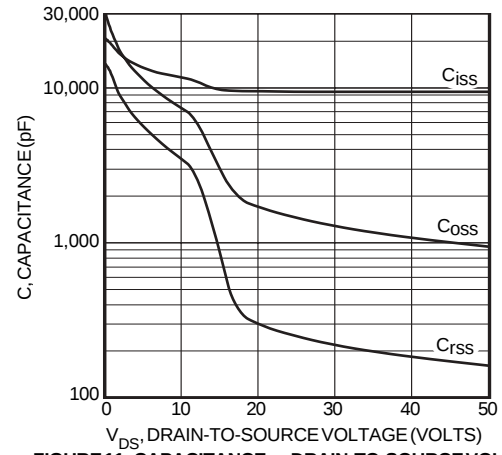


FIGURE 11, CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

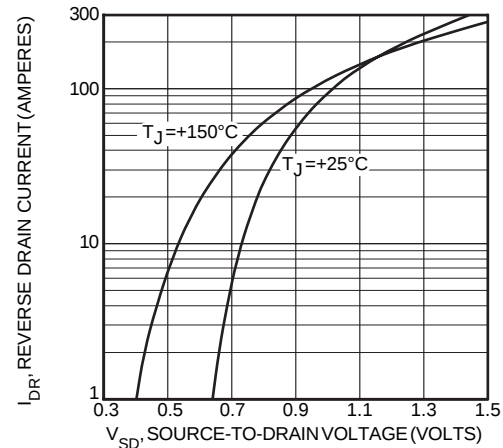


FIGURE 13, SOURCE-DRAIN DIODE FORWARD VOLTAGE

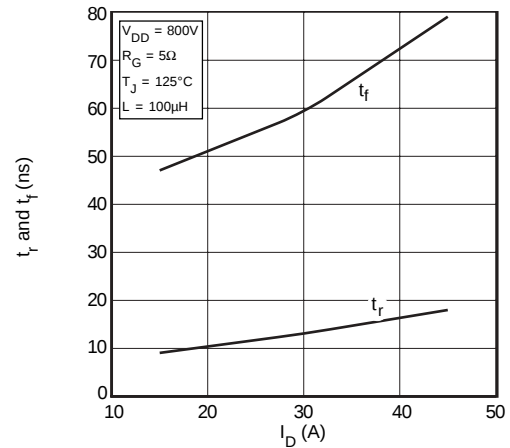


FIGURE 15, RISE AND FALL TIMES vs CURRENT

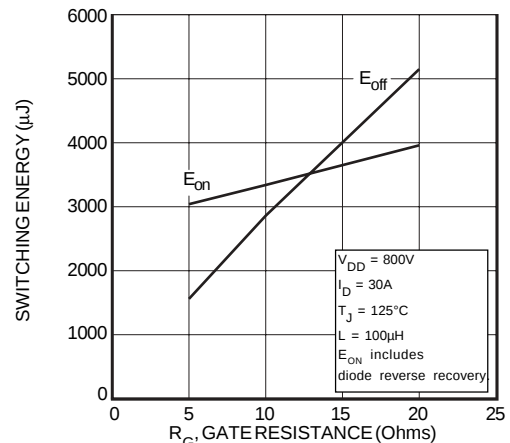


FIGURE 17, SWITCHING ENERGY vs. GATE RESISTANCE

A: 5.00 V
 A: 10.0ms
 W: 40 V
 M1 Area
 3.015mVps
 $T_J = 125\text{ C}$

10%
 t_{on}
 t_r
 90%
 5%
 10%
 5%
 Switching Energy

Gate Voltage
 Drain Current
 Drain Voltage

11 May 2003
 12:23:43

APT12031JFLL

Task 1: 500V/s

582 A/cm

90%

$t_{d(off)}$

Gate Voltage

2+

Drain Voltage

Drain Current

90%

10%

0

t_r

Switching Energy

Ch1: 500V 500ms Ch2: 10.0V 100ms Ch3: 10.0V 100ms

Math1: 1000ms

18 May 2023 11:28:31

Top View Dimensions:

- Overall width: 31.5 (1.240) / 31.7 (1.248)
- Distance between mounting holes: 7.8 (.307) / 8.2 (.322)
- Radius: $r = 4.0 (.157)$ (2 places)
- Distance from mounting hole to center of gate: 14.9 (.587) / 15.1 (.594)
- Distance between gate terminals: 30.1 (1.185) / 30.3 (1.193)
- Overall length: 38.0 (1.496) / 38.2 (1.504)

Side View Dimensions:

- Lead height: 11.8 (.463) / 12.2 (.480)
- Lead thickness: 8.9 (.350) / 9.6 (.378)
- Distance from lead to mounting hole: 4.0 (.157) / 4.2 (.165) (2 places)
- Distance from mounting hole to center of gate: 3.3 (.129) / 3.6 (.143)
- Distance from mounting hole to center of drain: 1.95 (.077) / 2.14 (.084)
- Distance from mounting hole to center of source: 12.6 (.496) / 12.8 (.504)
- Overall height: 25.2 (0.992) / 25.4 (1.000)

Detail View Dimensions:

- Gate terminal width: 0.75 (.030) / 0.85 (.033)
- Source terminal width: 0.75 (.030) / 0.85 (.033)

Other Labels:

- W=4.1 (.161) / W=4.3 (.169) / H=4.8 (.187) / H=4.9 (.193) (4 places)
- Hex Nut M4 (4 places)
- * Source
- Drain
- * Source
- Gate

* Source terminals are shorted internally. Current handling capability is equal for either Source terminal.

APT's products are covered by one or more of U.S. patents 4,895,810 5,045,903 5,089,434 5,182,234 5,019,522 5,262,336 6,503,786 5,256,583 4,748,103 5,283,202 5,231,474 5,434,095 5,528,058 and foreign patents. US and Foreign patents pending. All Rights Reserved.