Application Note:

LR1110 Evaluation Kit

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1 Introduction

LR1110 is a long range, ultra-low power transceiver aimed to enhance LoRa-based geolocation applications. In addition to Wi-Fi and GNSS geolocation capabilities, it supports LoRa® and (G)FSK modulations, and is fully compatible with previous generations of LoRa radios. It is able to transmit either up to +22dBm on the High-Power PA, or up to +15dBm on the Low Power TX path, and supports a continuous low power operation in the 150MHz-960MHz ISM bands.

This application note aims at helping engineers understanding the functionalities of the LR1110 Evaluation Kit. It also provides a deep description of the LR1110 reference design, and gives guidelines for a successful implementation of the LR1110 device in the end application.

It is recommended to read this application note in conjunction with the following documents:

- LR1110 Datasheet
- LR1110 User Manual

2 LR1110 Evaluation Kit Description

Figure 1: LR1110 Evaluation Kit

The LR1110 Evaluation kit is composed of:

- 2x LR1110 shields
  - PCB E516V02B, equipped with an integrated GNSS LNA for passive antenna applications
  - PCB E592V01B, without GNSS LNA for active antenna usage
- 1x STM32L476RG Nucleo board
- 1x TFT touch screen
- 1x GNSS active antenna with SMA connection
- 1x GNSS passive antenna with SMA connection
- 1x 2.4GHz antennas with SMA connection
- 1x region specific sub-GHz antenna with SMA connection (915 MHz, 868 MHz or 490 MHz frequency bands)

3 LR1110 Shield Schematic Description

The LR1110 evaluation boards (E516V02B or E592V01B) feature GNSS and Wi-Fi sniffing path, in addition to a sub-GHz RF path. All three RF paths are terminated with SMA connectors for easy antenna or RF equipment connection.

3.1 Schematic Overview

The complete electrical schematic of the LR1110 evaluation kit is depicted hereafter (E516V02B PCB). Each portion is described in dedicated sections.

The LR1110 RF section appears in the red box. The additional sections are dedicated to connections with the STM32L476RG Nucleo kit or test points.

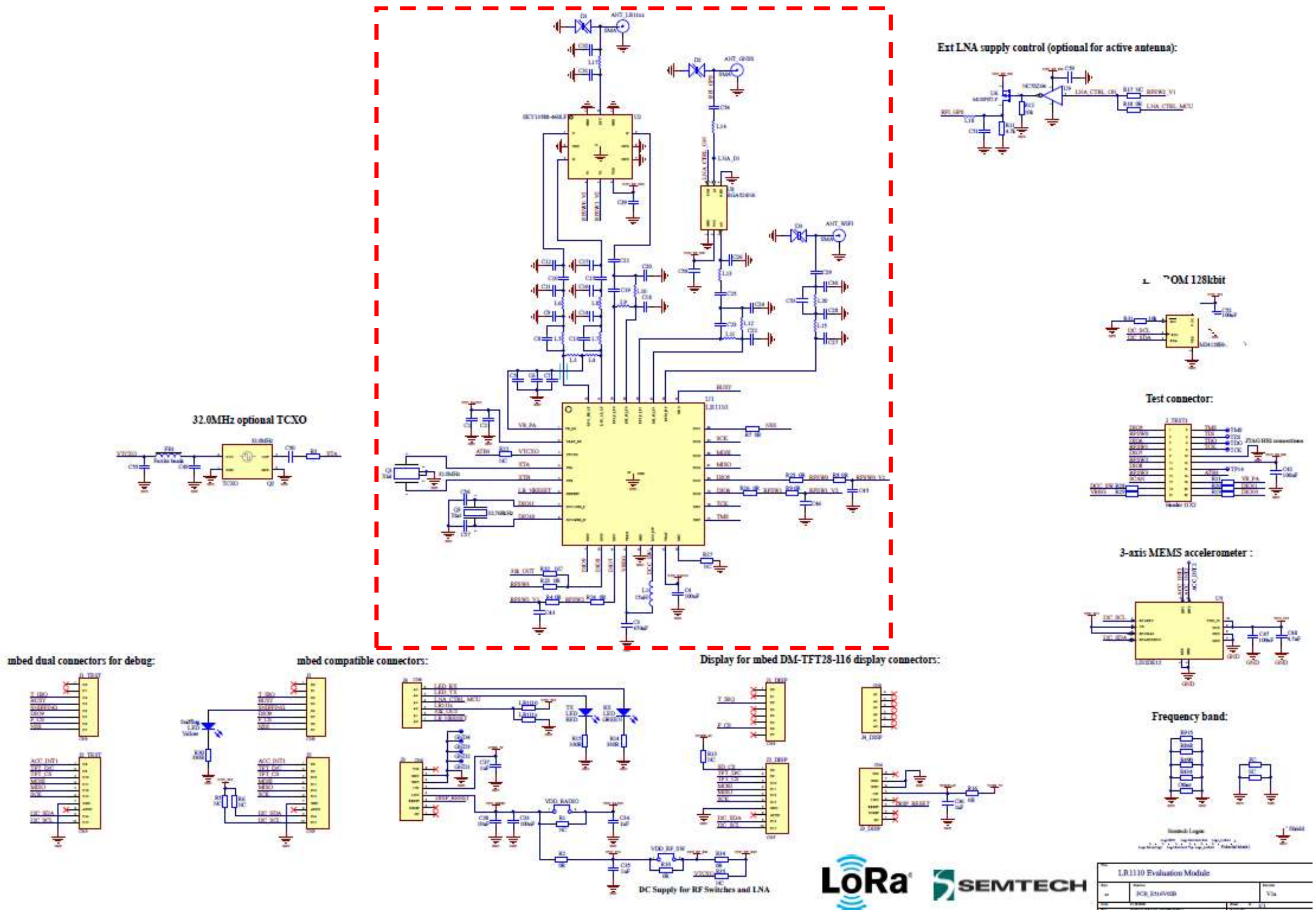

Figure 2: LR1110 Eval Kit Schematic Overview (E516V02B PCB)

3.2 Sub-GHz Path

The sub-GHz path is implemented in a multi-band configuration. It uses both the High Power PA (+22dBm) on the RFO_HP_LP pin and the Low Power PA (+15dBm) on the RFO_HP_LP pin. Therefore, two different configurations targeting different frequency bands with different output power requirements can be implemented on a single PCB. Both PAs are combined with the sub-GHz RX path using a SKY13588 SP3T RF switch, allowing optimized performance on both TX and RX paths compared to a single tie implementation.

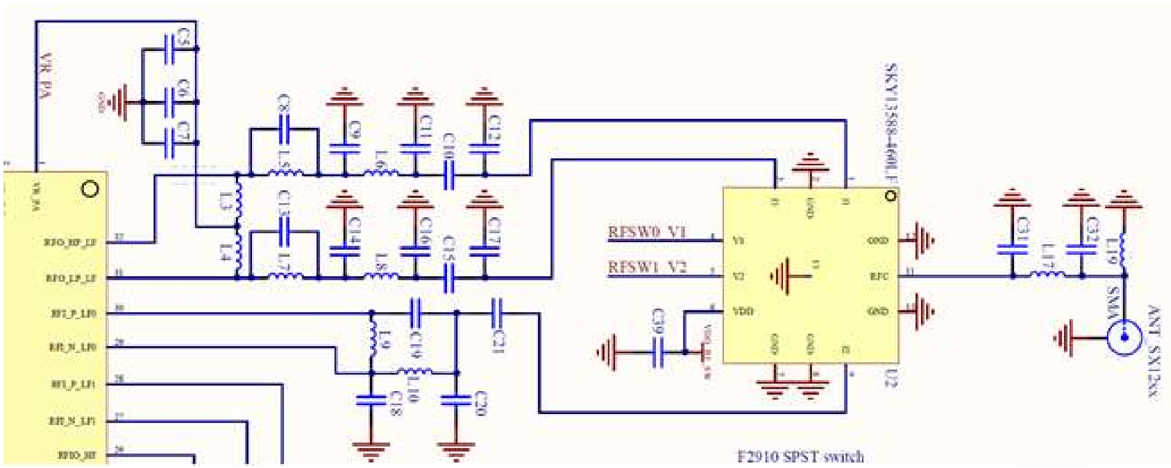

Figure 3: Sub-GHz Path

3.2.1 PA Matching Network Structure

Both PA paths have the common structure:

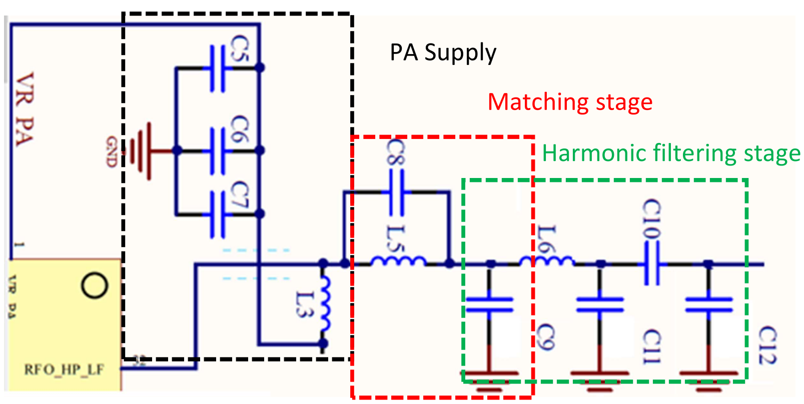

Figure 4: PA Matching Network Structure

Each PA is supplied from the VR_PA pin through a 47nH LQW choke inductor (L3). The VR_PA path shall be carefully decoupled (C5, C6, C7), ideally using NP0 capacitors. Special care has to be put on the design of this section to minimize the harmonic radiations, actually minimizing the length of the VR_PA line.

The matching network aims at presenting the optimum load Zopt at the PA output pin in order to generate the maximum output power at the operating frequency, with the highest efficiency (therefore the minimum power consumption), while minimizing the PA harmonic components.

The matching network is composed of 2 sections:

- the impedance matching stage, aims at presenting the Zopt load at the PA pin
- the harmonic filtering stage allows a low pass filtering in order to reduce the level of PA harmonics, and then comply with the regulatory requirements.

An additional harmonic filtering stage can be implemented after the RF switch if required (C31/L17/C32 pi section in Figure 3: Sub-GHz Path). It is advised to implement this additional filter by default in the design, and to let it unpopulated (nc/0R/nc) if no additional filtering is necessary.

Please note that a serial capacitance (C10) is required to remove the PA DC component to protect the RF switch.

3.2.2 PA Matching Network Component Values

Each one of the PA matching network is also implemented in a multiband global matching, taking benefit of the LR1110 adaptive TX: one Bill Of Materials is defined for the higher frequency bands (850-928MHz), and another BOM for the 490MHz band. For each of those two bands, the component values are kept identical for the different frequencies.

The PA however always operates at the optimum configuration thanks to the adaptive TX: the PA parameters (TXPWR, PaDutyCycle, and PaHPSel) are adapted to the operating frequency, keeping the output power, efficiency and harmonic components at the optimized level for each frequency.

3.2.3 Single Band Operation

In case of a single band operation, only one PA pin would be used as input of the TX path (either RFO_HP_LF or RFO_LP_LF). The second and unused pin shall then be left open. In such a case, a SPDT RF switch can be used to combine the TX and RX paths to the antenna path.

3.2.4 RX Stage

The sub-GHz RX stage is implemented in a 4-elements differential structure on the RFI_N_LF0 and RFI_P_LF0 pins, with a use of a balun to adapt the differential to single transformation and the impedance matching. The single ended RX path is then connected to the RF switch together with the TX path (refer to Figure 3: Sub-GHz Path). This allows achieving the lowest noise figure on the RX stage, and therefore the best sensitivity figures. Please note that a serial capacitance (C21) is required to prevent DC components damaging the LR1110 RX stage.

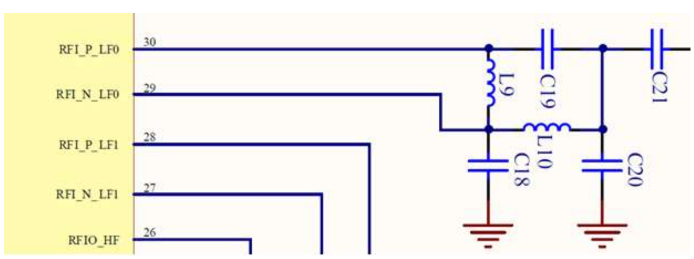

Figure 5: Sub-GHz RX Stage

3.3 GNSS Path

The LR1110 features a GNSS input path to allow geolocation for outdoor conditions.

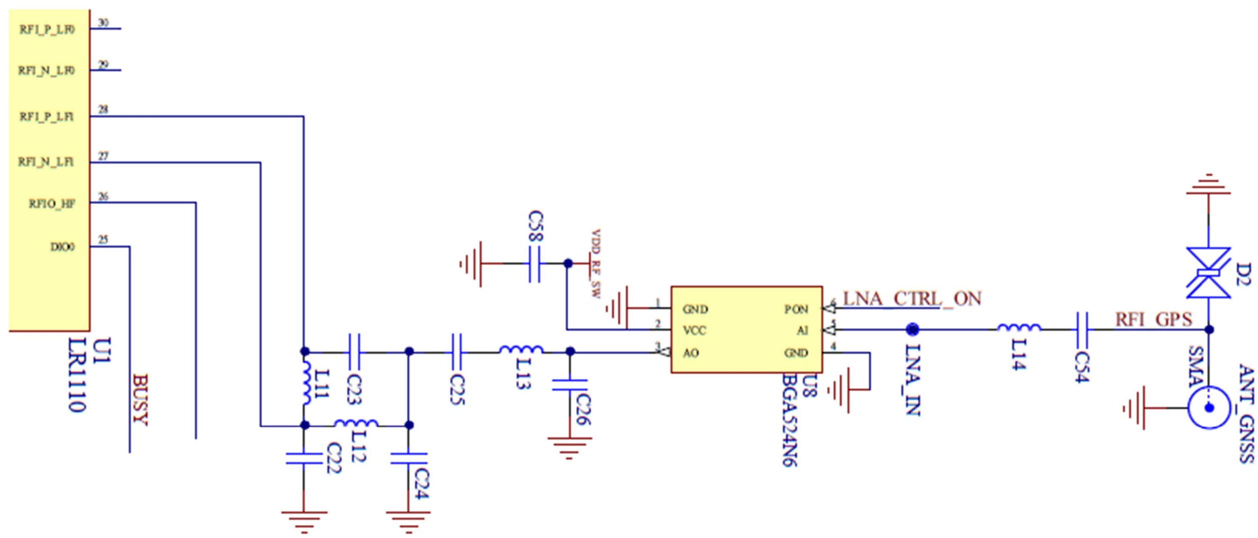

Figure 6: GNSS Path, E516V02B Shield with Embedded LNA

Similarly to the sub-GHz RX stage, the GNSS RX stage is implemented in a 4-elements differential structure on the RFI_N_LF1 and RFI_P_LF1 pins, with a use of a balun to adapt the differential to single transformation and the impedance matching (L11/L12/C22/C23/C24). This allows achieving the lowest noise figure on the RX stage, and therefore the best GPS reception performance. A first order low pass filter (L13/C26) provides additional RF filtering.

An external LNA is present on the RF path of the E516V02B PCB in order to allow optimum sensitivity performance in passive antenna implementations, as described in section 3.3.1 On-Board LNA. This LNA is bypassed on the E592V01B PCB, where an active antenna is used.

An additional TVS protection on the SMA connector (D2) allows protecting the BGA524N6 from Electrostatic Discharge on the antenna port.

3.3.1 On-Board LNA

The E516V02B PCB is equipped with an Infineon BGA524N6 Low Noise Amplifier, allowing a passive antenna implementation. This LNA is supplied on VDD_RF_SWITCH, a power supply rail shared with the RF switches and different from the LR1110 power supply. It is controlled by the LNA_CTRL_ON, connected to either the STM32L476 Nucleo pins (LNA_CTRL_MCU), or by the LR1110 itself (RFSW2, connected to DIO7) using 0 Ohm assembly options, as shown in Figure 8: LNA Supply on the GNSS Path here below.

3.3.2 Active Antenna

The other LR1110 shield (E592V01B) is dedicated to use cases with an active antenna. Since the active antenna already integrates a GNSS LNA, the LNA on the E592V01B LR1110 shield PCB is bypassed.

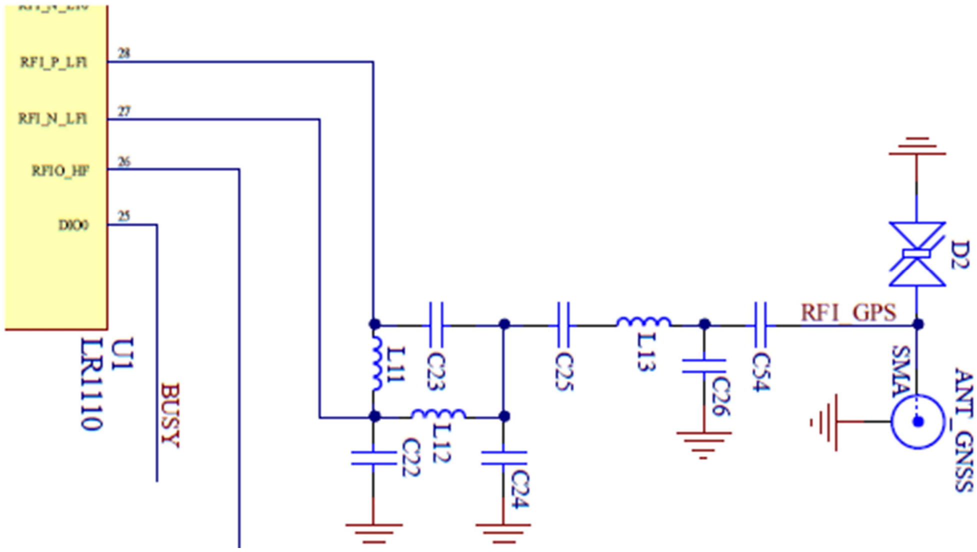

Figure 7: GNSS Path, E592V01B Shield without LNA

The LR1110 Evaluation Kit provides a 3.3V voltage on the RF line of the GNSS path. An additional power source is therefore not required in order to supply an active antenna or another LNA directly screwed on the LR1110 GNSS SMA connector. The active antenna supply is activated by the on-board LNA control pin LNA_CTRL_ON, and is therefore controlled to either the STM32L476 Nucleo pins (LNA_CTRL_MCU), or by the LR1110 itself (RFSW2, connected to DIO7) using 0 Ohm assembly options, as shown in Figure 8: LNA Supply on the GNSS Path here below.

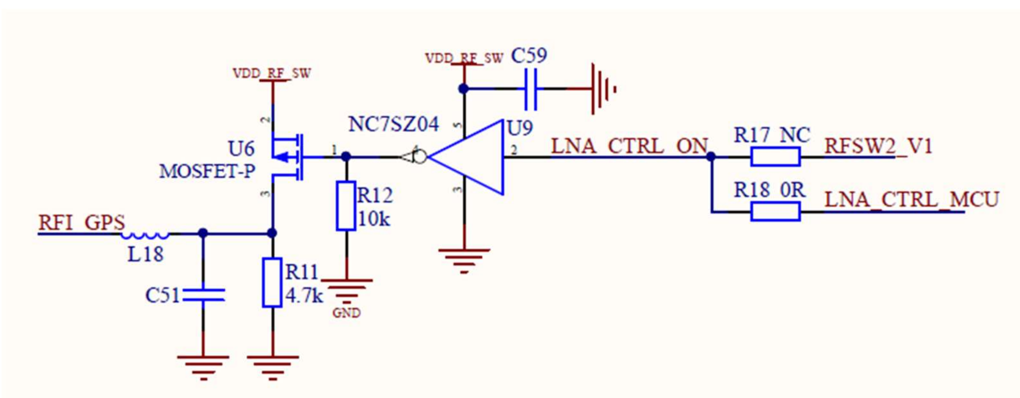

Figure 8: LNA Supply on the GNSS Path

3.4Wi-Fi Path

The LR1110 also features a Wi-Fi input path to allow geolocation e.g. for indoor conditions.

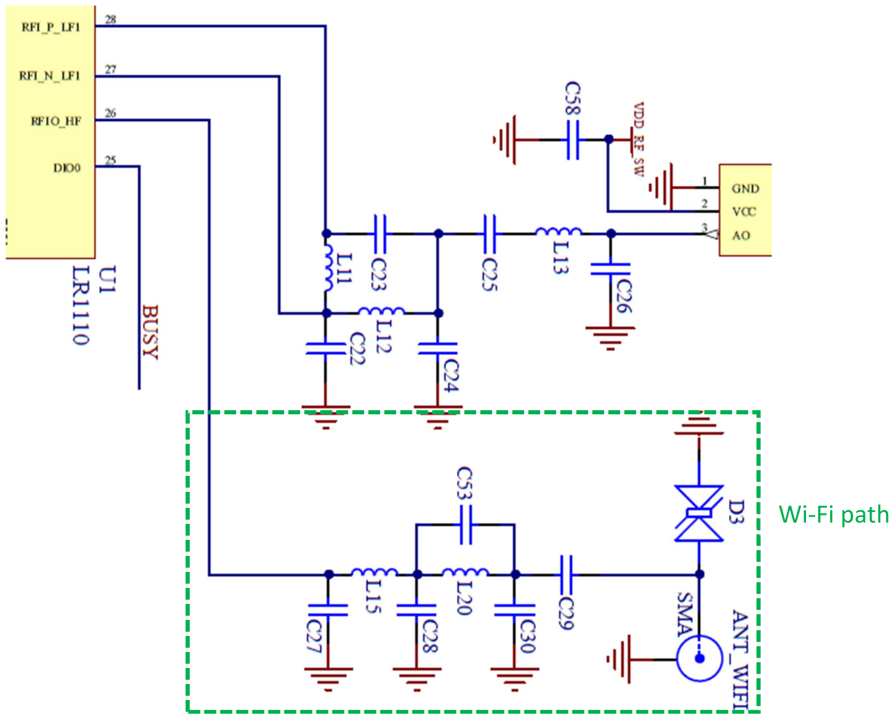

Figure 9: Wi-Fi Path

The Wi-Fi RX stage output has a single-ended implementation on the RFIO_HF pin. The SMD components on this path aim at providing additional RF filtering. Please note that a serial capacitance (C29) is required to prevent DC components injected on the antenna port damaging the LR1110 Wi-Fi stage.

An additional TVS protection on the SMA connector (D3) allows protecting the BGA524N6 from Electrostatic Discharge on the antenna port.

3.5 Oscillators

32 MHz and 32.768 kHz oscillators are implemented in the LR1110 Evaluation Kit. The LR1110 supports either a 32 MHz crystal oscillator, or a TCXO. Both oscillator sources are implemented in the LR1110 reference design in order to provide design guidance.

A 32 MHz TCXO and a 32.768 kHz crystal oscillator are mandatory for GNSS applications.

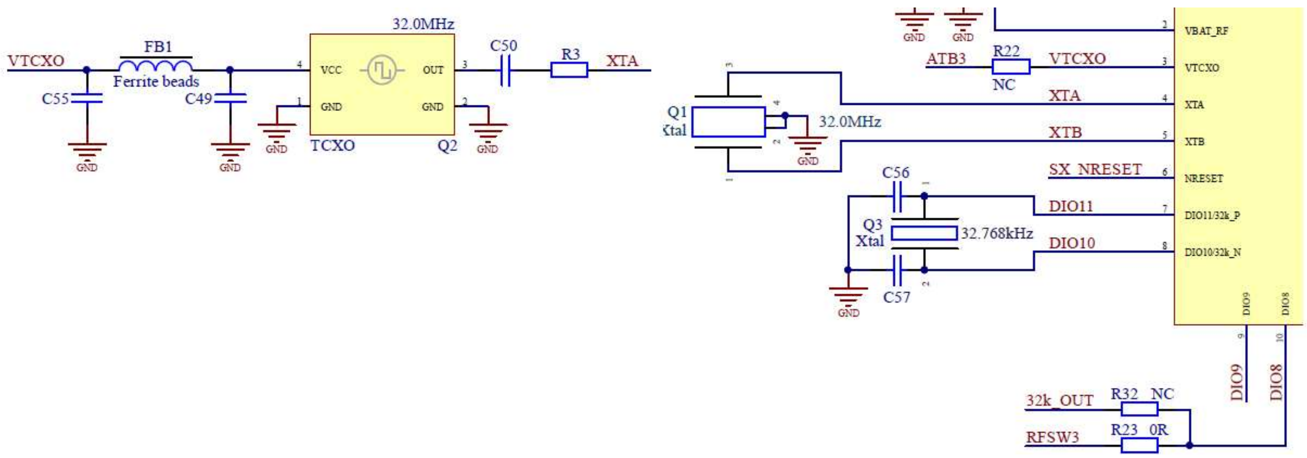

Figure 10: LR1110 Oscillators

Special care has to be given on the design of the 32 MHz crystal oscillator section: it is advised to implement a thermal relief to guarantee best operation even in case of the 32 MHz crystal oscillator self-heating due to extended TX operation. Please refer to the AN1200.37 “Recommendations for Best Performance” for details.

DIO8 has a double function on the LR1110: it can either control the external RF Switches, or can be used to feed a 32.768 kHz signal to the host, in order for the system to support only a single 32.768 kHz crystal oscillator, and therefore reduce the BOM cost. By default, the LR1110 is used connected to the node RFSW3 of J_TEST1 connector. R23 and R32 assembly option allows connecting DIO8 to the Arduino signal A1 of J4/CN8 connector.

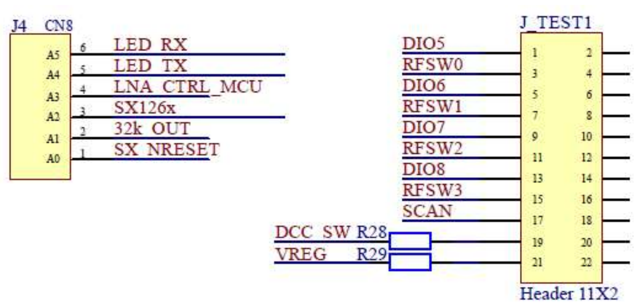

Figure 11: DIO8 Connections

3.6 Power Management

The LR1110 Evaluation Kit is supplied directly by the STM32L476RG Nucleo board. Therefore, the LR1110 Evaluation Kit can be supplied via USB from a PC or a power bank. The usage of the STM32L476RG Nucleo board power management allows keeping the LR1110 Evaluation Kit power management to its minimum, such as in an end application.

The LR1110 supports two power supply modes: either a DC-DC configuration for lowest power consumption, or a LDO configuration for a reduced Bill Of Materials. Inductor L1 (15uH) indicates that the LR1110 Evaluation Kit is implemented in a DC-DC configuration. However, it is also possible to evaluate the LDO configuration keeping the L1 inductor via LR1110 user commands. L1 can be removed in case of a LDO implementation in the end application.

The VDD_RADIO signal is the main power supply line of the LR1110.

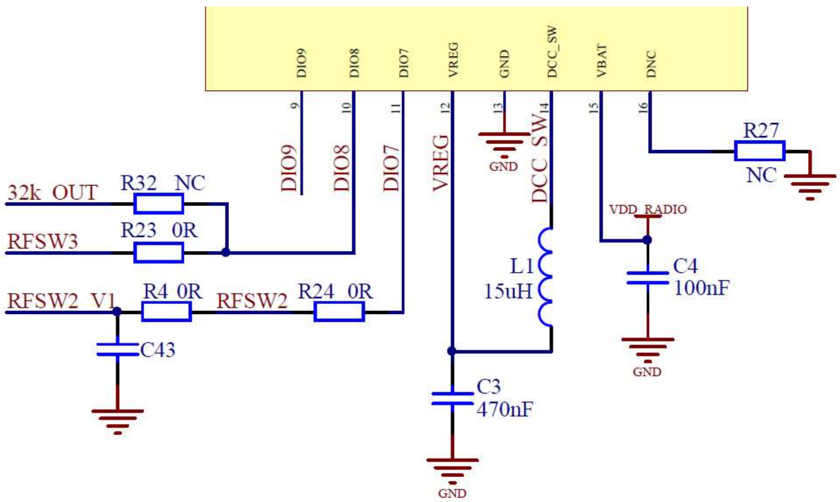

Figure 12: Power Management in DC-DC Configuration

Special care has to be given on the design of the DC-DC inductor section: it is advised to implement the DCC_SW to VREG loop as short as possible and with the lowest serial resistance, in order to ensure the highest DC-DC converter efficiency, and therefore the lowest power consumption during the DC-DC operation.

3.7 Semtech Test Signals

Some LR1110 test signals reserved for Semtech are accessible on the LR1110 Evaluation Kit, as shown in Figure 13: Test Functions on 16, 17, 18 and 24. Those functionalities are not necessary for a regular usage of the LR1110, and therefore shall not be implemented in an application:

- Pin 16 DNC shall be left “Not Connected”, therefore R27 is not necessary.
- Pin 17 DNC shall be left “Not Connected”.
- Pin 18 DNC shall be left “Not Connected”.
- Pin 24 DIO1 shall be directly connected to the NSS signal (R7 shall be 0R value)

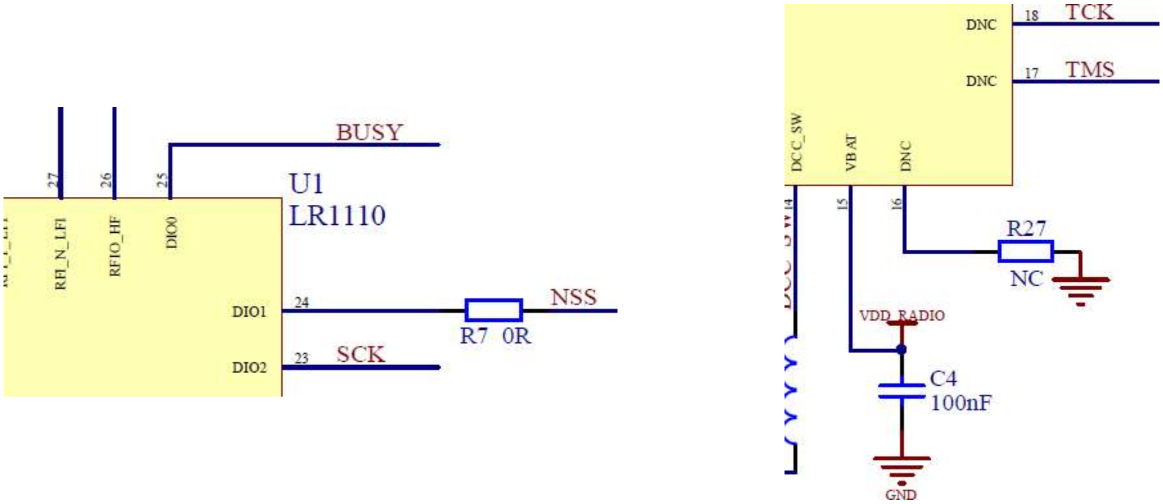

Figure 13: Test Functions on 16, 17, 18 and 24

3.8 LED

Two LED (green and red) on the LR1110 Evaluation kit allow monitoring the sub-GHz RX and TX operations. An additional yellow LED is dedicated for GPS and Wi-Fi sniffing indication.

Those LEDs are controlled by the STM32L476RG Nucleo, and therefore are freely available to the user.

3.9 Test Points

Numerous test points are available on the evaluation kit, allowing to monitor the LR1110 power consumption or voltage levels, or also to give access to the STM32L476RG Nucleo pins for debug or evaluation purpose.

The LR1110 current consumption can be monitored on the VDD_RADIO jumper. An additional jumper connector VDD_RF_SW is dedicated to monitoring the RF switches current consumption.

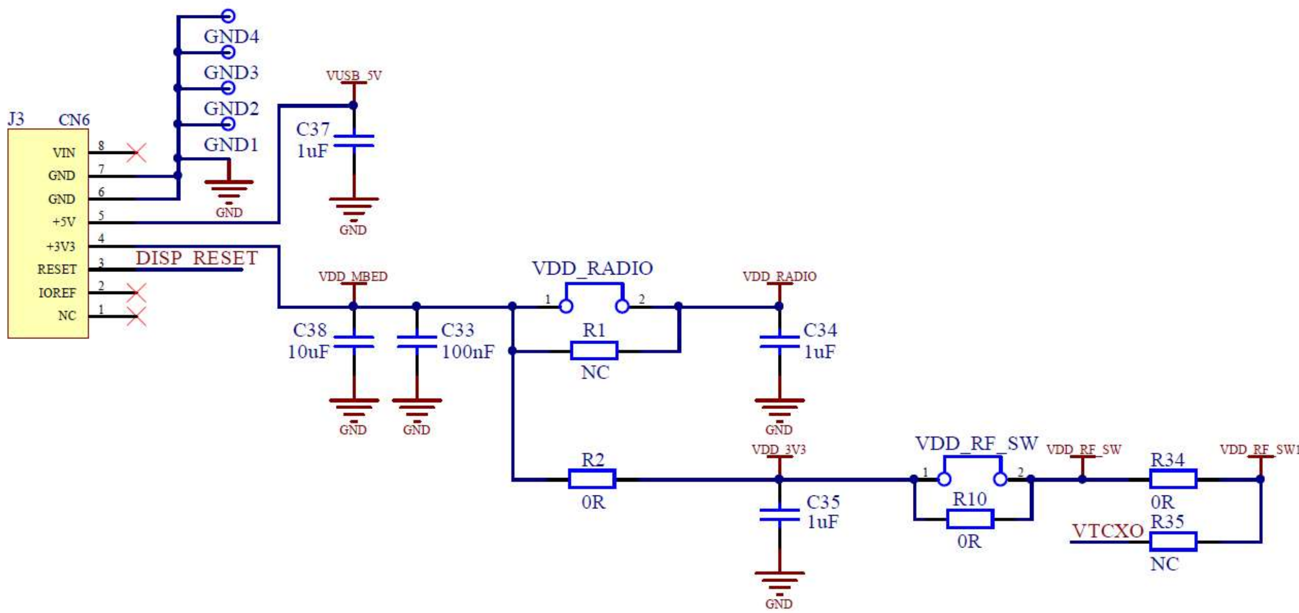

Figure 14: LR1110 and RF Switches Power Supply Connectors

J_TEST1 connector gives access to the DCC_SW, VREG, VR_PA , DIO10 and DIO11 pins though the R28, R29, R21, R20 and R19 assembly options respectively. Please note that those resistors assembled by default on the LR1110 kit.

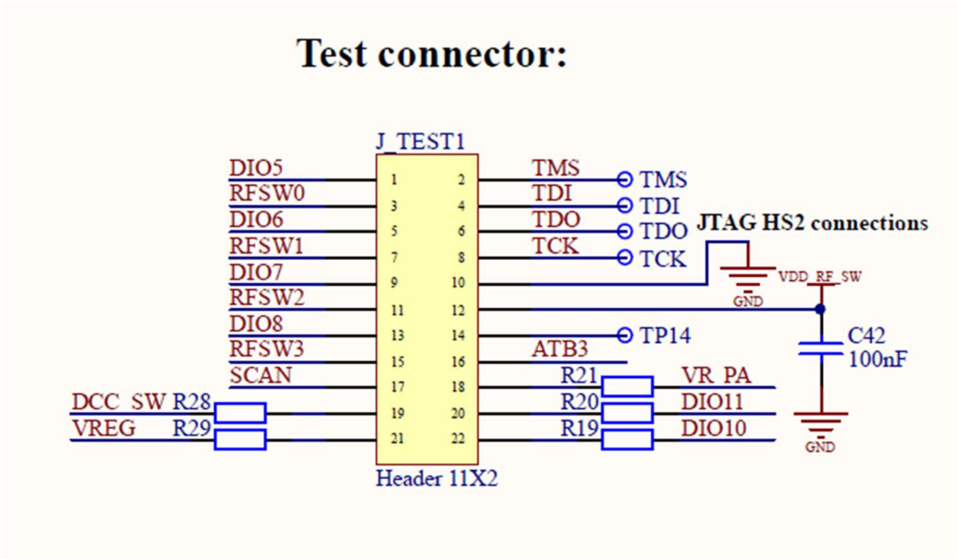

Figure 15: J_TEST1 Connector

The SP3T RF switch is controlled by the LR1110. J-TEST1 also provides the flexibility to control them from the Nucleo board if desired.

J1_TEST1 and J_TEST2 connectors provide access to the STM32L476RG Nucleo SPI and I2C pins.

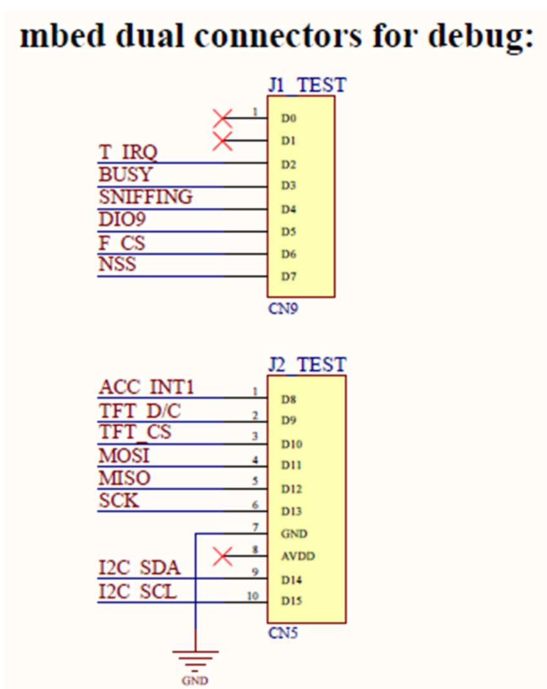

Figure 16: J1_TEST and J2_TEST Nucleo Test Connectors

4 PCB Layout

This LR1110 Evaluation Kit was designed on a low-cost, standard four-layer FR-4 substrate. The top layer houses all of the components and critical RF layout. The IN1 layer serve as continuous ground plane to ensure optimum RF performance. The IN2 and BOT are used as control signals and power supply routing.

To mitigate the impact of reference frequency drift on receive performance due to high heat dissipation of the LR1110 during sub-GHz TX operation, extra precautions were taken to isolate the crystal from the rest of the PCB on all layers. As shown in Figure 17 to Figure 20, a copper void around the reference was implemented on all layers.

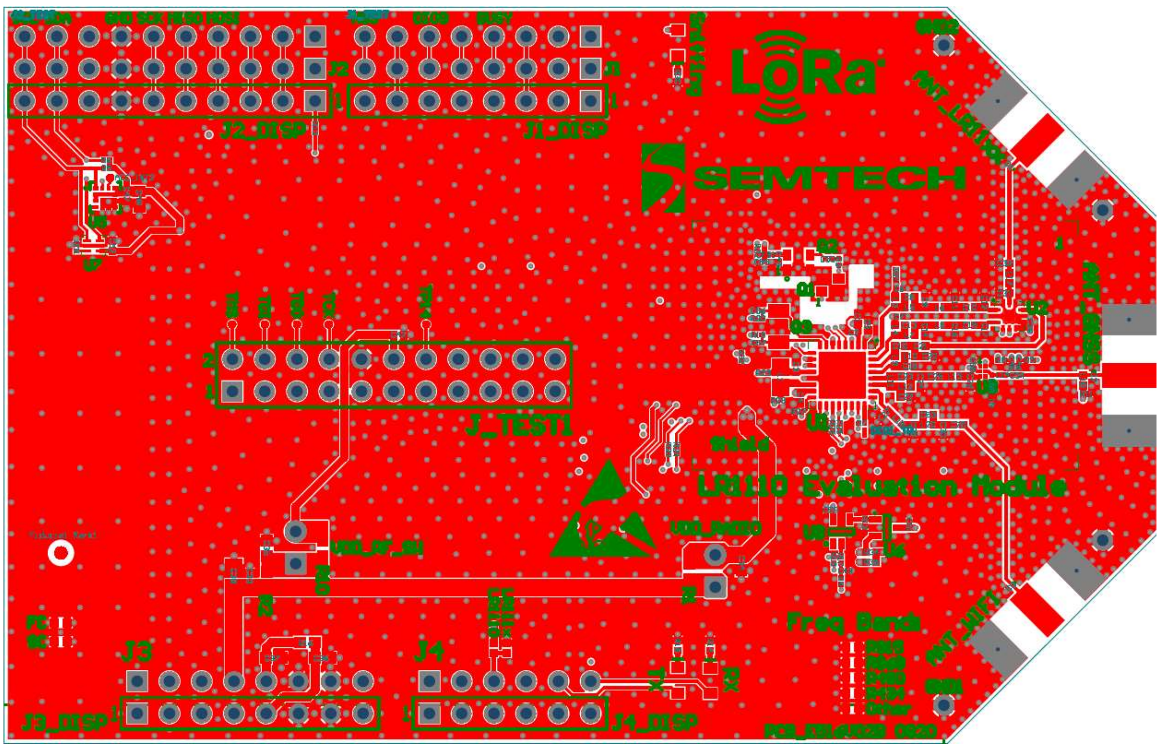

Figure 17: LR1110 Evaluation Kit TOP Layer (E516V02B)

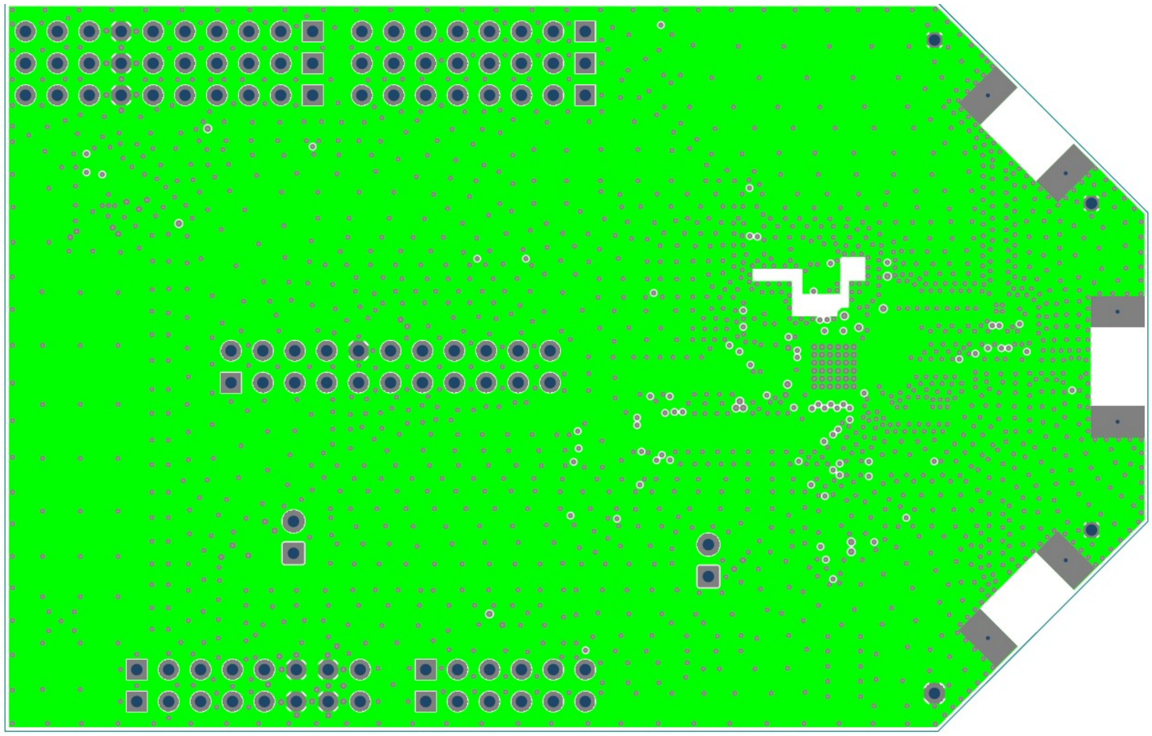

Figure 18: LR1110 Evaluation Kit IN1 Layer (E516V02B)

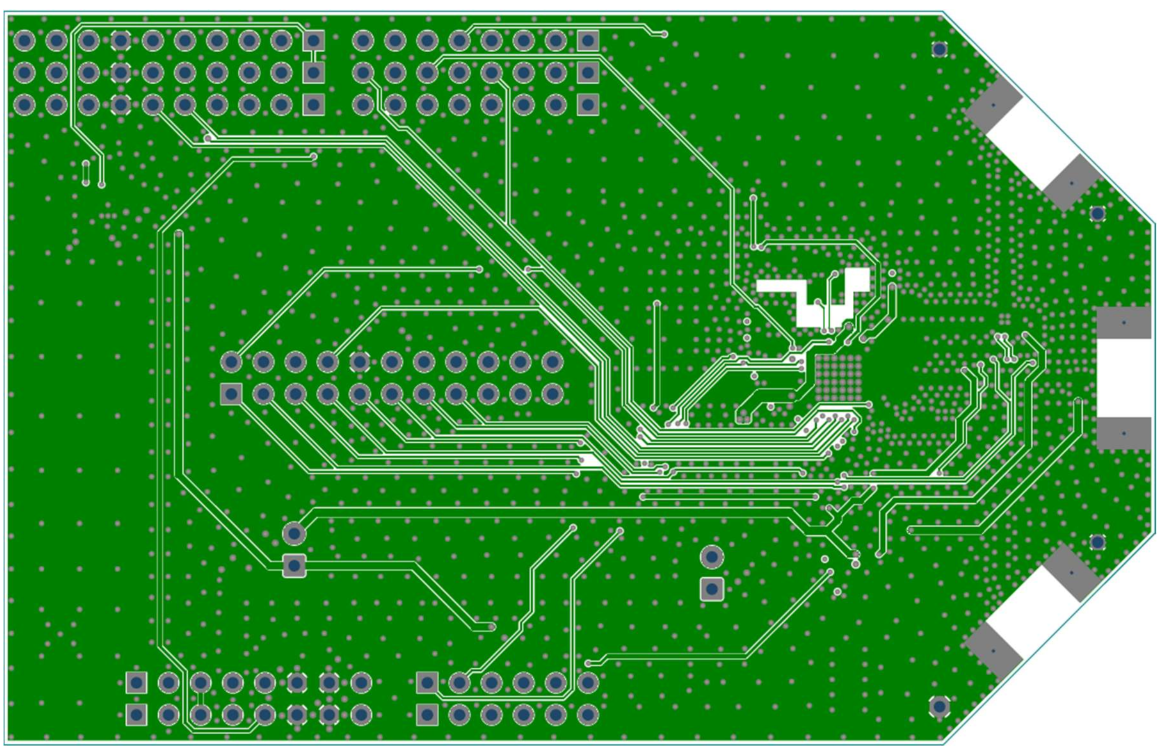

Figure 19: LR1110 Evaluation Kit IN2 Layer (E516V02B)

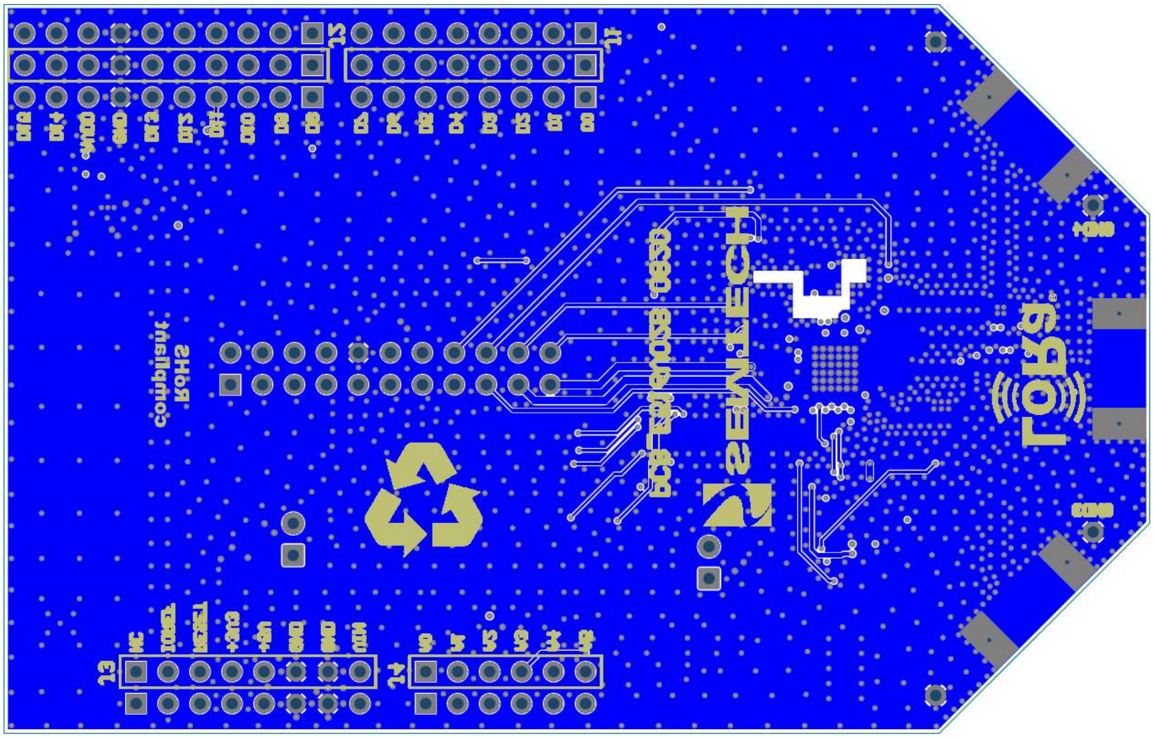

Figure 20: LR1110 Evaluation Kit BOT Layer (E516V02B)

5 Revision History

Version	Date	Modifications
1.0	February 2020	Initial Release
1.1	March 2020	Typo corrections

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