CMOSTEK CMT2189B

240 – 960 MHz SoC OOK Transmitter

Features

- High-Performance RISC CPU
  - PIC16-likeInstruction-set
  - Only 37 instructions to learn:
    - All Single-Cycle Except Branches
  - Operating speed:
    - Up to 16 MHz Clock
    - 125nsinstruction cycle
    - F_{SYS} = 8MHz @ 2.0V~3.6V
    - F_{SYS} = 16MHz @ 2.7V~3.6V
  - Interrupt capability
  - 8-level deep hardware stack
  - 2048 Words Flash / 128B SRAM / 256B EEPROM
  - 2 x 8-bit timers/counters with programmable prescaler
  - 8 I/O pins with individual direction control:
    - Interrupt-on-pin change
    - Individually programmable weak pull-ups
    - Push-pull output except PA5
- High-Performance OOK Transmitter
  - All Features Configurable
  - Frequency Range: 240 to 960 MHz
  - OOK Modulation
  - Symbol Rate up to 40 kbps
  - Single-Ended PA Output
  - Output Power: 0 to +13 dBm
- Supply Voltage: 2.0 to 3.6 V
- FCC / ETSI Compliant
- RoHS Compliant

Applications

- Remote Keyless Entry (RKE)
- Garage and gate door openers
- Home/Building Automation and Security
- Industrial Monitoring and Controls
- Remote Lighting Control
- Wireless Alarm and Security Systems
- Consumer Electronics Applications

Descriptions

The CMT2189B devices are fully integrated, highly flexible, high performance, SoC OOK transmitters with embedded RISC microcontroller core for various 240 to 960 MHz wireless applications. They are part of the CMOSTEK NextGenRF™ family, which includes a complete line of transmitters, receivers and transceivers. The CMT2189B uses a 1-pin crystal oscillator circuit with the required crystal load capacitance integrated on-chip to minimize the BOM counts. The device can deliver up to +13 dBm output power and the single-ended PA output. The device operates from 2.0 V to 3.6 V. Its low power design enables superior operation life for battery powered application. The CMT2189B transmitter together with CMOSTEK NextGenRF™ receiver enables a highly flexible, low cost RF link.

Ordering Information

Part Number	Frequency	Package Option	MOQ
CMT2189B-ESR	433.92 MHz	T&R	2,500 pcs
CMT2189B-ESB	433.92 MHz	Tube	1,000 pcs
More Ordering Info: See Page 30			

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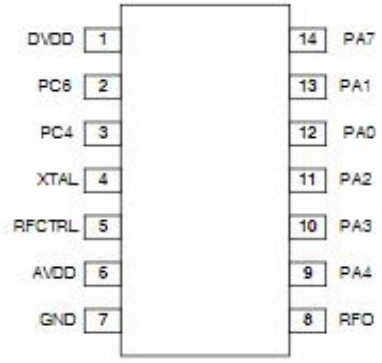


CMT2189B Pin Arrangement

Typical Application

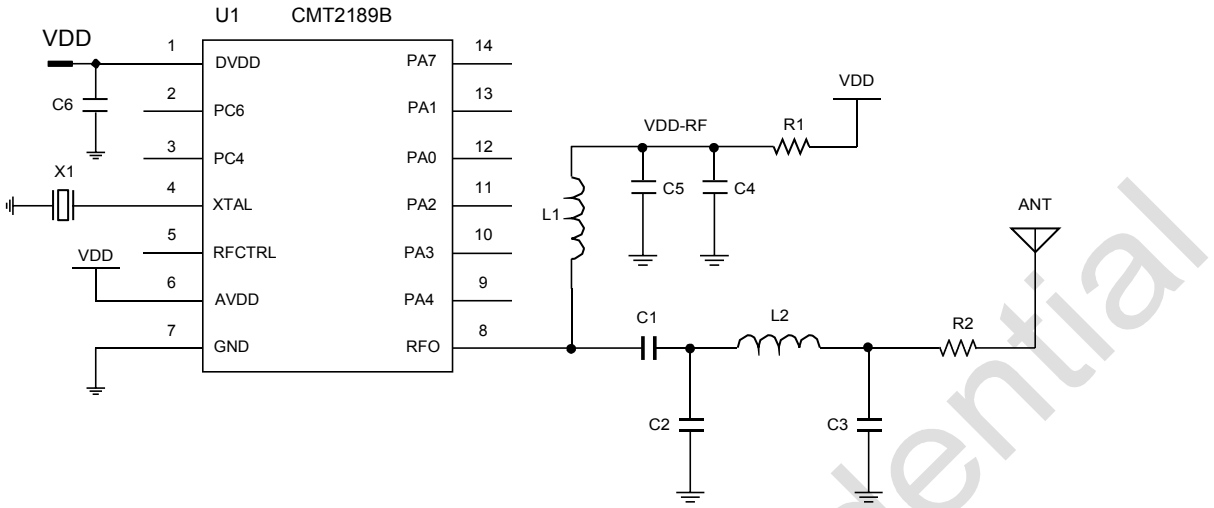


Figure 1.CMT2189B Typical Application with Single-Ended PA Output

Table 1.BOM of 315/433.92 MHz Application with Single-Ended PA Output

Designator	Descriptions	Value 315MHz	Value 433.92MHz	Unit	Manufacturer
U1	CMT2189B, 240 – 960 MHz SoC OOK transmitter		-	-	CMOSTEK
X1	±20 ppm, SMD32*25 mm crystal	26.25	26.2982	MHz	EPSON
L1	±10%, 0603 multi-layer chip inductor	220	180	nH	Sunlord
L2	±10%, 0603 multi-layer chip inductor	33	27	nH	Sunlord
C1	±0.25 pF, 0402 NP0, 50 V	82	68	pF	
C2	±0.25 pF, 0402 NP0, 50 V	2	NC	pF	
C3	±0.25 pF, 0402 NP0, 50 V	NC	2.2	pF	
C4	±0.25 pF, 0402 NP0, 50 V	470		pF	
C5	±20%, 0603 X7R, 25 V	0.1		uF	
C6	±20%, 0603 X7R, 25 V	0.1		uF	
R1	±5%, 0402	10		Ω	
R2	±5%, 0402	10		Ω	

Abbreviations

Abbreviations used in this data sheet are described below

AN	Application Notes
BOM	Bill of Materials
BSC	Basic Spacing between Centers
BW	Bandwidth
DC	Direct Current
EEPROM	Electrically Erasable Programmable Read-Only Memory
ESD	Electro-Static Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
FSK	Frequency Shift Keying
GFSK	Gauss Frequency Shift Keying
GUI	Graphical User Interface
IC	Integrated Circuit
LDO	Low Drop-Out
Max	Maximum
MCU	Microcontroller Unit
Min	Minimum
MOQ	Minimum Order Quantity
NP0	Negative-Positive-Zero
OBW	Occupied Bandwidth
OOK	On-Off Keying
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PLL	Phase Lock Loop
PN	Phase Noise
RBW	Resolution Bandwidth
RCLK	Reference Clock
RF	Radio Frequency
RFPDK	RF Product Development Kit
RoHS	Restriction of Hazardous Substances
Rx	Receiving, Receiver
SOT	Small-Outline Transistor
TBD	To Be Determined
Tx	Transmission, Transmitter
Typ	Typical
XO/XOSC	Crystal Oscillator
XTAL	Crystal

Table of Contents

1. Electrical Characteristics

V_{DD} = 3.3 V, T_{OP} = 25 ℃, F_{RF} = 433.92 MHz, OOK modulation, output power is +10 dBm terminated in a matched 50 Ω impedance with single-ended PA output, unless otherwise noted.

1.1 Recommended Operating Conditions

Table 2. Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operation Voltage Supply	V_{DD}		2.0		3.6	V
Operation Temperature	T_{OP}		-40		85	℃
Supply Voltage Slew Rate			1			mV/us

1.2 Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings[1]

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}		-0.3	3.6	V
Interface Voltage	V_{IN}		-0.3	V_{DD} +0.3	V
Junction Temperature	T_J		-40	125	℃
Storage Temperature	T_{STG}		-50	150	℃
Soldering Temperature	T_{SDR}	Lasts at least 30 seconds		255	℃
ESD Rating		Human Body Model (HBM)	-2	2	kV
Latch-up Current		@ 85 ℃	-100	100	mA

Note:

[1]. Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

1.3 Transmitter Specifications

Table 4. Transmitter Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Frequency Range	F_{RF}		240		960	MHz
Symbol Rate	SR	OOK	0.5		40	ksps
Output Power	P_{OUT}		0		+13	dBm
Output Power Step Size	P_{STEP}			1		dB
Current Consumption, Single-ended	$I_{DD-S-315}$	0 dBm, 50% duty cycle		3.2		mA
		+10 dBm, 50% duty cycle		7.0		mA
		+13 dBm, 50% duty cycle		8.0		mA
	$I_{DD-S-434}$	0 dBm, 50% duty cycle		3.5		mA
		+10 dBm, 50% duty cycle		7.5		mA
		+13 dBm, 50% duty cycle		8.6		mA
	$I_{DD-D-868}$	0 dBm, 50% duty cycle				mA
		+10 dBm, 50% duty cycle				mA
		+13 dBm, 50% duty cycle				mA
	$I_{DD-D-915}$	0 dBm, 50% duty cycle				mA
		+10 dBm, 50% duty cycle				mA
		+13 dBm, 50% duty cycle				mA
Sleep Current	I_{SLEEP}			1		uA
Phase Noise @434	PN_{434}	100 kHz offset from F_{RF}		-80		dBc/Hz
		200 kHz offset from F_{RF}		-83		dBc/Hz
		400 kHz offset from F_{RF}		-91		dBc/Hz
		600 kHz offset from F_{RF}		-96		dBc/Hz
		1.2 MHz offset from F_{RF}		-105		dBc/Hz
Phase Noise @868MHz	PN_{868}	100 kHz offset from F_{RF}		-77		dBc/Hz
		200 kHz offset from F_{RF}		-79		
		400 kHz offset from F_{RF}		-87		
		600 kHz offset from F_{RF}		-91		dBc/Hz
		1.2 MHz offset from F_{RFI}		-100		dBc/Hz
Harmonics Output for 315 MHz	$H2_{315}$	2nd harm @ 630 MHz, +13 dBm P_{OUT}		< -45		dBm
	$H3_{315}$	3rd harm @ 945 MHz, +13 dBm P_{OUT}		< -45		dBm
Harmonics Output for 434 MHz	$H2_{434}$	2nd harm @ 868MHz, +13 dBm P_{OUT}		< -45		dBm
	$H3_{434}$	3rd harm @ 1302 MHz, +13 dBm P_{OUT}		< -45		dBm
Harmonics Output for 868 MHz	$H2_{868}$	2nd harm @ 1736 MHz, +13 dBm P_{OUT}		< -36		dBm
	$H3_{868}$	3rd harm @ 2604 MHz, +13 dBm P_{OUT}		< -36		dBm
Harmonics Output for 915 MHz	$H2_{915}$	2nd harm @ 1830 MHz, +13 dBm P_{OUT}		< -36		dBm
	$H3_{915}$	3rd harm @ 2745 MHz, +13 dBm P_{OUT}		< -36		dBm
OOK Extinction Ration				60		dB

1.4 RF Crystal Oscillator

Table 5. Crystal Oscillator Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Crystal Frequency	$F_{XTAL315}$			26.25		MHz
	$F_{XTAL433.92}$			26.2982		
	$F_{XTAL868}$			26.303		
	$F_{XTAL915}$					
Crystal Tolerance[1]				±20		ppm
Load Capacitance	C_{LOAD}			15		pF
Crystal ESR	Rm				60	Ω
XTAL Startup Time[2]	t_{XTAL}			400		us

Notes:

[1]. This is the total tolerance including (1) initial tolerance, (2) crystal loading, (3) aging, and (4) temperature dependence. The acceptable crystal tolerance depends on RF frequency and channel spacing/bandwidth.

[2]. This parameter is to a large degree crystal dependent.

1.5 Internal High Frequency Oscillator

Table 6. IHRC Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
IHRC Frequency	F_{IHRC}	3.3V, 27℃		15.99		MHz
Temperature-dependent		-20℃~ +80℃, 3.3V		4.2%/100℃		
Voltage-dependent		2~3.6V		±3		%/V
Setup Time				2.2	10	us
Leakage Current				0.8	2	nA
Triming Range		Step 0.625%		±20%		

1.6 Internal Low Frequency Oscillator

The ILRCsupport two frequency: 32KHz or 256KHz. It can be selected by LFMOD in OSCCON register, 0 is the 32KHz, and the 1 is the 256KHz.

Table 7. ILRC Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ILRC Frequency	F_{ILRC}	2.5V, 25℃, 32K		32.3		KHz
		2.5V, 25℃, 256K		258.5		KHz
Temperature-dependent		-20℃~ +80℃, 2.5V		22.3%/100℃		
Voltage-dependent		2~3.6V		±11.1		%/V
Setup Time		2.5V, 25℃		4.6	10	us
Leakage Current		Disable		0.15	1	nA

1.7 LVD/LVR

Table 8. LVD/LVR Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LVD Voltage				2.0		V
				2.2		
				2.8		
LVR delay				125	157	us

1.8 POR

Table 9. POR Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POR Current	I_{POR}	3.3V		50		nA
Temperature-dependent		3.3V		2.0		V

1.9 I/O PAD

Table 10. I/OPAD Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Low Voltage	VIL				0.3	VDD
Input High Voltage	VIH		0.7			VDD
Output High Current	I_{OH}	3.3V, 25℃		10		mA
Output Low Current	I_{OL}	3.3V, 25℃		15		mA
Weak Pull-up		3.3V		41.7		KΩ

1.10 MCU Supply Current

Table 11. Supply Current

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operation Mode		3.3V, F_{SYS} = 2MHz		310		uA
		3.3V, F_{SYS} = 32KHz		50		uA
Sleep Mode with WDT_ON		3.3V		3		uA
Sleep Mode with WDT_OFF		3.3V		0.8		uA
Sleep Mode with LVD_ON		3.3V		15		uA
Notes: 1. All the IO is input mode, and with pull-down resistance. 2.Comparator is disable, CM<2:0> = 111						

2. Pin Descriptions

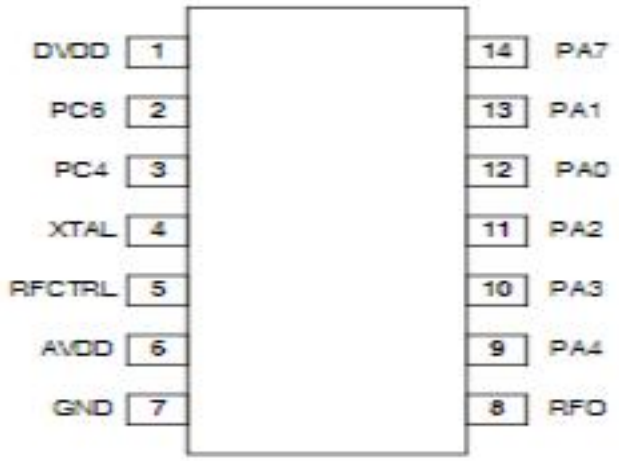


Table 12. CMT2189B Pin Descriptions

Pin Number	Name	I/O	Descriptions	
1	DVDD	I	MCU power supply input	
2	PC6	IO	PORTC I/O	
3	PC4	IO	PORTC I/O	
4	XTAL	I	single-ended crystal oscillator input or external reference clock input	
5	RFCTRL	I	RF's SPI interface enable control, internally pulled up to VDD, low active	
6	AVDD	I	RF power supply input	
7	GND	I	Ground	
8	RFO	O	The singled-ended power amplifier output	
9	PA4	IO	PORTA I/O w/programmable pull-up and interrupt-on-change	
10	PA3	IO	PORTA I/O w/programmable pull-up and interrupt-on-change	
11	PA2/T0CKI/INT	IO	PA2	PORTA I/O w/programmable pull-up and interrupt-on-change
			T0CKI	Timer0 clock input
			INT	External Interrupt
12	PA0/ICSPCLK	IO	PA0	PORTA I/O w/programmable pull-up and interrupt-on-change
			ICSPCLK	Serial Programming and debugging Data I/O
13	PA1/ICSPDAT	IO	PA1	PORTA I/O w/programmable pull-up and interrupt-on-change
			ICSPDAT	Serial Programming and debugging Clock
14	PA7/CLKI	IO	PA7	PORTA I/O w/programmable pull-up and interrupt-on-change
			CLKI	External clock input/RC oscillator connection
Internal pin	PC0/RFDIN	IO	PC0	PORTC I/O
			RFDIN	RF data input
	PC1/SDIO	IO	PC1	PORTC I/O
			SDIO	RF's serial interface data input/output
	PC2/SCLK	IO	PC2	PORTC I/O
			SCLK	RF's serial interface clock input
	PC3/CSB	IO	PC3	PORTC I/O
			CSB	RF's serial interface select enable input

3. Typical Performance Characteristics

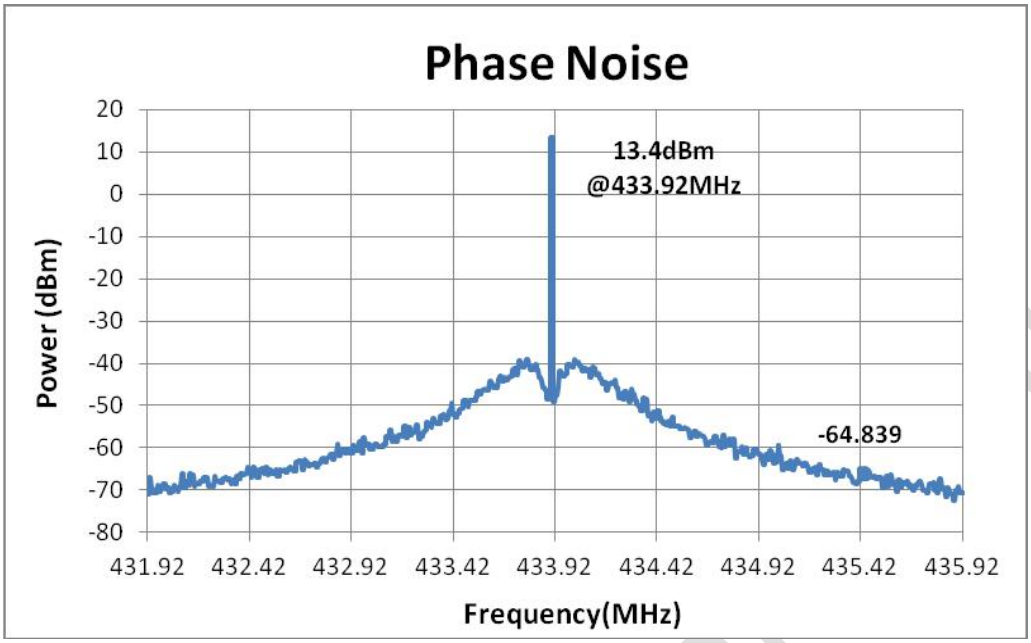


Figure 4. Phase Noise, F_{RF} = 433.92 MHz, P_{OUT} = +13 dBm, Single Carrier

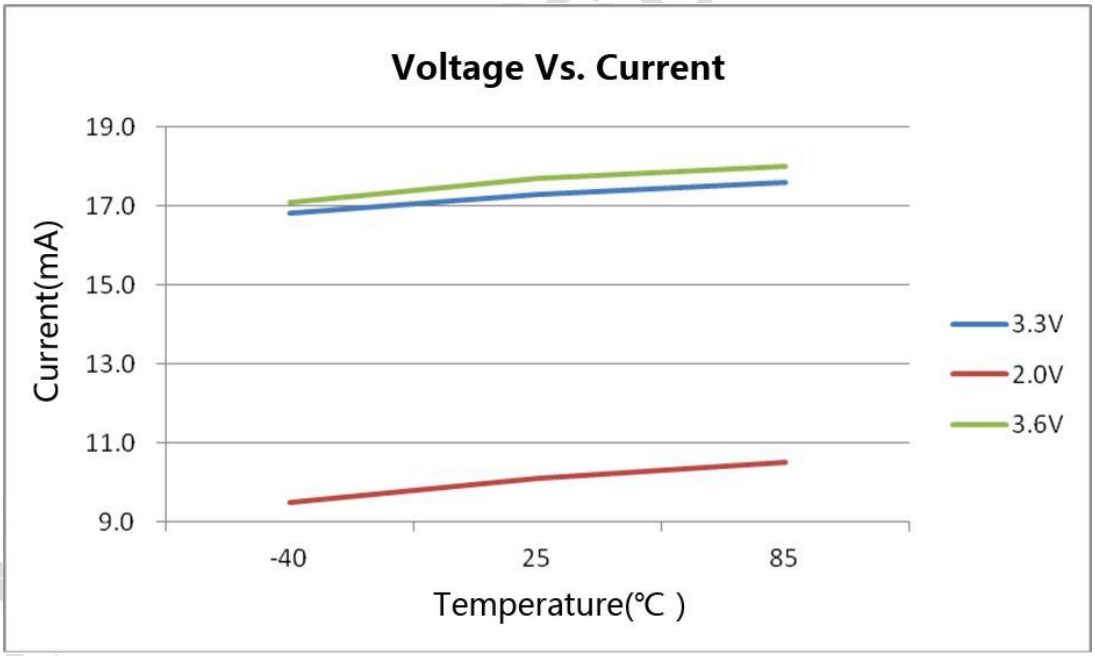


Figure 5. Tx power-Current-Voltage Characteristic Diagram

F_{RF} = 433.92 MHz, P_{OUT} = +13 dBm, Single Carrier (No Encoding)

4. Functional Descriptions

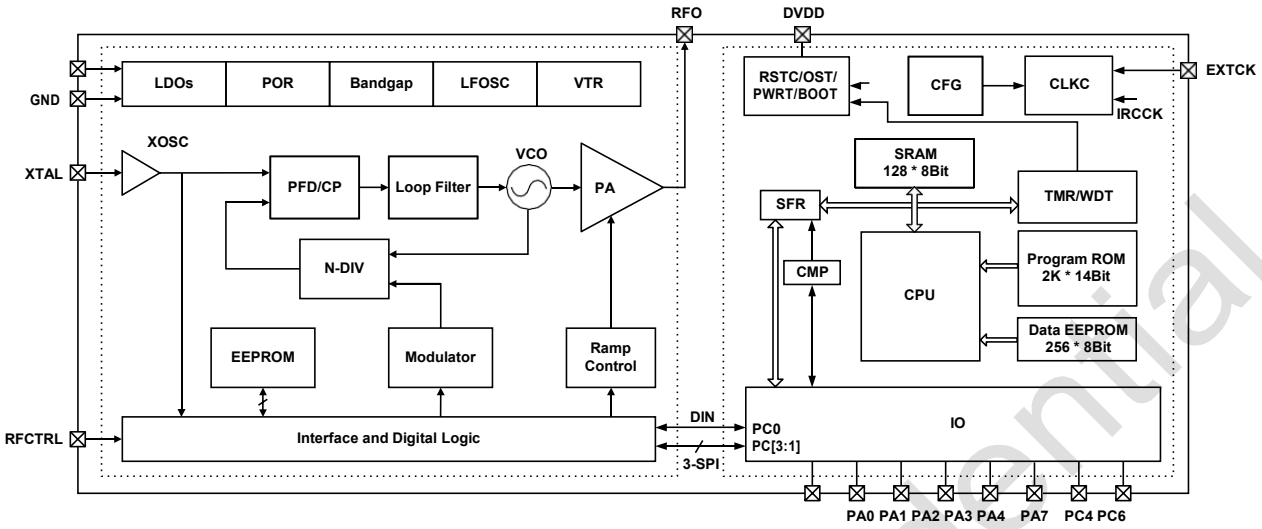


Figure 6. CMT2189B Functional Block Diagram

4.1 Overview

The CMT2189B devices are fully integrated, highly flexible, high performance, SoC OOK transmitters with an embedded RISC microcontroller designed for various 240 to 960 MHz wireless applications. They are part of the CMOSTEK NextGenRF™ family, which includes a complete line of transmitters, receivers and transceivers. The chip is optimized for the low system cost, low power consumption, battery powered application with its highly integrated and low power design.

The functional block diagram of the CMT2189B is shown in the figure above. The CMT2189B is based on direct synthesis of the RF frequency, and the frequency is generated by a low-noise integer-N frequency synthesizer. It uses a 1-pin crystal oscillator circuit with the required crystal load capacitance integrated on-chip to minimize the number of external components. Every analog block is calibrated on each Power-on Reset (POR) to the reference voltage generated by Bandgap. The calibration can help the chip to finely work under different temperatures and supply voltages. The CMT2189B has a highly efficient PA built in, the PA can be configured as single-ended outputs, and the output power can be configured from 0 to +13 dBm in 1 dB step size.

The RISC microcontroller has 2048-word flash program space. Up to 8 I/O are supported with their functions customized by the user program. RF Frequency, PA output power, other product features and unique transmit IDs can be programmed into the registers. This saves the cost and simplifies the product development and manufacturing effort. Alternatively, in stock products of 433.92 MHz is available for immediate demands. The CMT2189B operates from 2.0 to 3.6 V, only consumes 7.5 mA with 1527 format code, when transmitting +10 dBm power under 3.3 V supply voltage. The device together with CMOSTEK NextGenRF™ receiver enables a highly flexible, low cost RF link.

4.2 Modulation, Frequency, Deviation and Symbol Rate

The CMT2189B supports OOK modulation with the symbol rate up to 40 ksps. The CMT2189B continuously covers the frequency range from 240 to 960 MHz, including the license free ISM frequency band around 315 MHz, 433.92 MHz, 868.35 MHz and 915 MHz.

Table 13. Modulation, Frequency, Deviation and Symbol Rate

Parameter	Value	Unit
Modulation	OOK	-
Frequency	240 to 960	MHz
OOK Symbol Rate	0.5 to 40	ksps

4.3 Power Amplifier

A highly efficient Power Amplifier (PA) is integrated in the CMT2189B to transmit the modulated signal out. Depending on the application, the user can design a matching network for the PA to exhibit optimum efficiency at the desired output power for a wide range of antennas, such as loop or monopole antenna. Typical application schematics and the required BOM are shown in Page 2. For the schematic, layout guideline and the other detailed information please refer to “AN170 CMT2110/17B Schematic and PCB Layout Design Guideline” and “AN159 CMT211xB_215xL_B Transmit Matching Guideline”.

The output power of the PA can be configured by the user within the range from 0 dBm to +13 dBm in 1 dB step size, it can be configured by software using the RF’s SPI.

4.4 Crystal Oscillator and RCLK

The CMT2189B uses a 1-pin crystal oscillator circuit with the required crystal load capacitance integrated on-chip. Figure 7 shows the configuration of the XTAL circuitry and the crystal model. The recommended specification for the crystal is about 26 MHz with ±20 ppm, ESR (Rm) < 60 Ω, load capacitance C_{LOAD} ranging from 12 to 20 pF. To save the external load capacitors, a set of variable load capacitors C_L is built inside the CMT2189B to support the oscillation of the crystal.

To achieve the best performance, the user only needs to input the desired value of the XTAL load capacitance C_{LOAD} of the crystal (can be found in the datasheet of the crystal) to the RFPDK, then finely tune the required XO load capacitance according to the actual XO frequency.

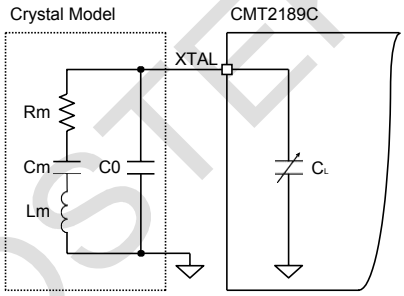


Figure 7. XTAL Circuitry and Crystal Model

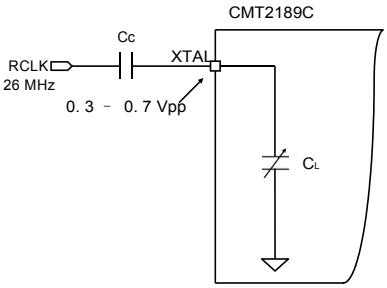


Figure 8. RCLK Circuitry

If a about 26 MHz RCLK (reference clock) is available in the system, the user can directly use it to drive the CMT2189B by feeding the clock into the chip via the XTAL pin. This further saves the system cost due to the removal of the crystal. A coupling capacitor is required if the RCLK is used. The recommended amplitude of the RCLK is 0.3 to 0.7 Vpp on the XTAL pin. Also, the user should set the internal load capacitor C_L to its minimum value. See Figure 8 for the RCLK circuitry.

5. RF Working States

The CMT2189B's RF has following 4 different working states: SLEEP, XO-STARTUP, TUNE and TRANSMIT.

SLEEP

When the CMT2189B is in the SLEEP state, all the internal blocks are turned off and the current consumption is minimized.

XO-STARTUP

Once the modulator of the CMT2189B detect valid signal on the D_{RAW} wire (see Figure 9), the RF section will go into the XO-STARTUP state, and the internal XO starts to work. The user has to wait for the t_{XTAL} to allow the XO to get stable. The t_{XTAL} is to a large degree crystal dependent. A typical value of t_{XTAL} is provided in the Table.

TUNE

The frequency synthesizer will tune the CMT2189B to the desired frequency in the time t_{TUNE}. The PA can be turned on to transmit the data only after the TUNE state is done, before that the data will not be transmitted. See the figure below for for the details.

TRANSMIT

The CMT2189B starts to modulate and transmit the data (D_{RAW}) generated by the microcontroller core responding to the push buttons, and as well as using the RF's SPI to send go_tx command. The transmission can be ended in 2 methods: firstly, driving the DATA pin low for t_{STOP} time, where the t_{STOP} is 20 ms; secondly, issuing sleep command over the RF's SPI interface, this will stop the transmission immediately. More details for how to use the CMT2189B, please see "AN201 CMT2189B User Guide".

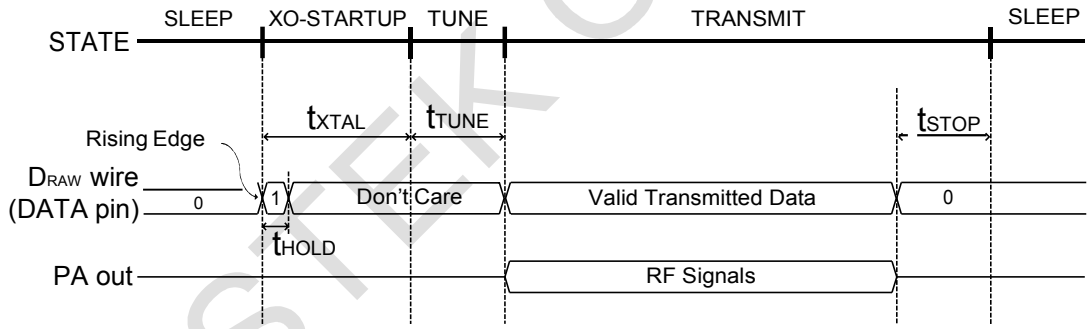


Figure 9. Transmission Enabled by DATA Pin Rising Edge

Table 14. Timing in Different Working States

Parameter	Symbol	Min	Typ	Max	Unit
XTAL Startup Time [1]	t_{XTAL}		400		us
Time to Tune to Desired Frequency	t_{TUNE}		370		us
Hold Time After Rising Edge	t_{HOLD}	10			ns
Time to Stop The Transmission	t_{STOP}		20		ms

Notes:
[1]. This parameter is to a large degree crystal dependent.

6. RISC Microcontroller Core

The embedded high-performance RISC Microcontroller has the following features:

High-Performance RISC CPU

- 2048 words Flash ROM, 128B SRAM
- 256B EEPROM
- All single-cycle instructions except branches
- Operating Speed
  - DC - 16MHz oscillator
  - 125 ns instruction cycle
- Interrupt Capability
- 8-Level Deep Hardware Stack
- Power-Saving Sleep mode
- Power-on Reset (POR)
- Multiplexed MCLRB/Input Pin

Peripheral Features

- 8 I/O Pins
  - Individual Direction Control
  - Interrupt-on-Pin Change
  - Individual Programmable Weak Pull-ups
- Timer0: 8-bit timer with 3-bit prescaler
- Timer2: 8-bit timer with 3-bit prescaler
- Watchdog timer with on-chip RC oscillator

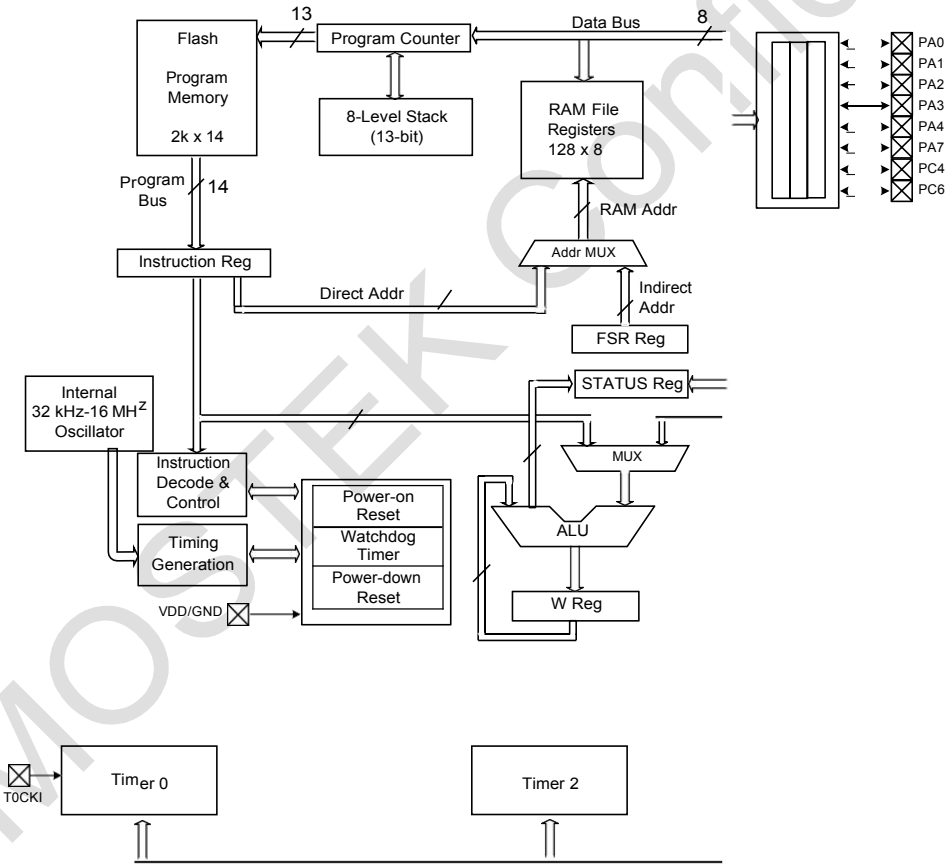


Figure 10. Microcontroller Core Block Diagram

6.1 Memory Organization

6.1.1 Program Memory Organization

The CMT2189B device has 2k x 14 (0000h-07FFh) space for program memory. Accessing a location above these boundaries will cause a wrap-around within the first 2k x 14 space. The Reset Vector is at 0000h and the Interrupt Vector is at 0004h (see figure below).

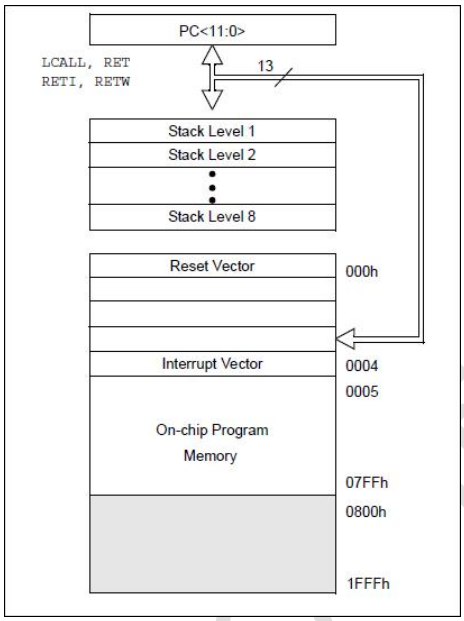


Figure 113. Program Memory Map and Stack

6.1.2 Data Memory Organization

The data memory (see figure 11) is partitioned into two banks: The General-Purpose Registers and the Special Function Registers. The Special Function Registers are located in the first 32 locations of each bank. Register locations 20h-5Fh are General Purpose Registers, implemented as static RAM and are mapped across both banks. All other RAM is unimplemented and returns '0' when being read. PAGE(STATUS<5>) is the bank select bit.

- PAGE0 = 0 Bank 0 is selected.
- PAGE0 = 1 Bank 1 is selected.

6.1.2.1 General Purpose Register File

The register file is organized as 64 x 8 in theCMT2189B. Each register is accessed, either directly or indirectly, through the FSR.

6.1.2.2 Special Function Register File

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device. These registers are static RAM. The special registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the "core" are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

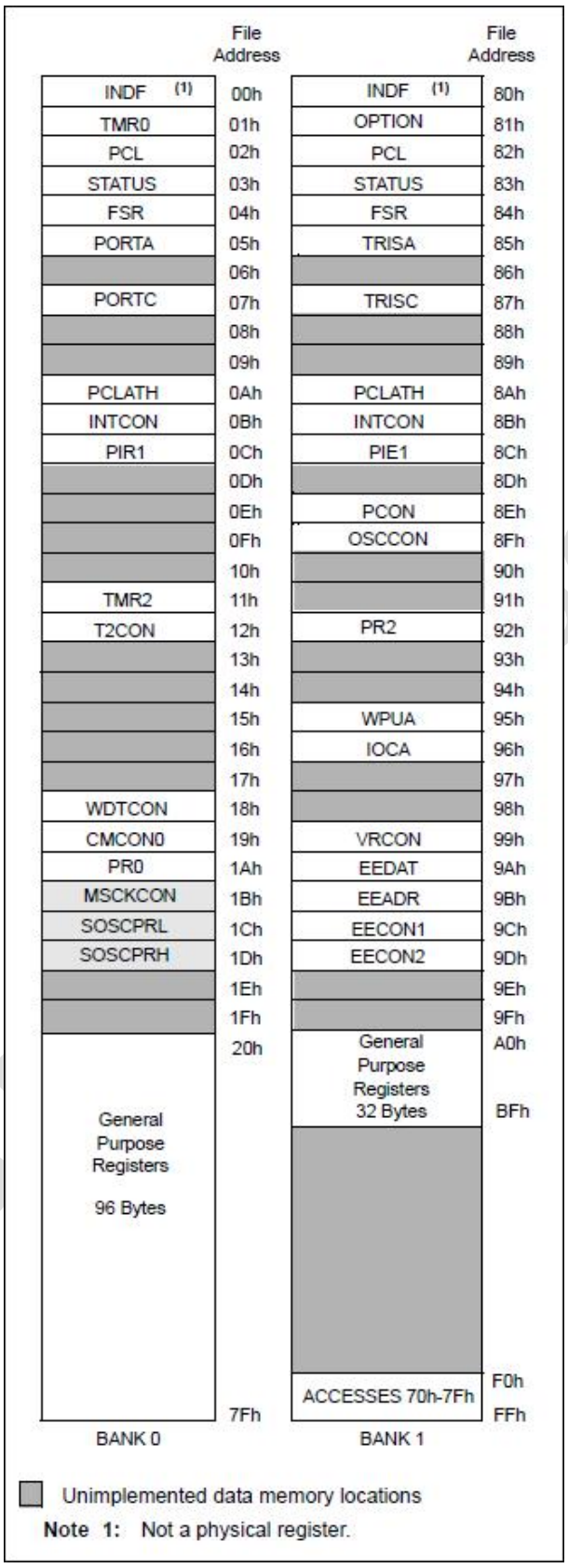


Figure 124. Data Memory Map of the CMT2189B

Table 15. CMT2189B Special Registers Summary Bank0

ADDR	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	POR reset
0	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								x x x x x x x x
1	TMR0	Timer0 Module's register, Timer0<7:0>								x x x x x x x x
2	PCL	Program Counter's (PC) Least Significant Byte, PC<7:0>								0000 0000
3	STATUS	-	-	PAGE	/TF	/PF	Z	HC	C	-- 01 1 x x x
4	FSR	Indirect Data Memory Address Pointer								
5	PORTA	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	00x0 0000
6										- - - - - - - -
7	PORTC	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	0000 0000
8										- - - - - - - -
9										- - - - - - - -
A	PCLATH	-	-	-	Write Buffer for upper 5 bits of Program Counter, PC<13:8>					--- 0 0 0 0 0
B	INTCON	GIE	PEIE	T0IE	INTE	PAIE	T0IF	INTF	PAIF	0000 0000
C	PIR1	EEIF	CKMEAIF	-	C2IF	C1IF	OSFIF	TMR2IF	-	00 - 0 000 -
D										- - - - - - - -
E										- - - - - - - -
F										- - - - - - - -
10										- - - - - - - -
11	TMR2	Timer2 Module register, Timer2<7:0>								0000 0000
12	T2CON	-	TOUTPS<3:0>				TMR2ON	T2CKPS<1:0>		- 000 0000
13										- - - - - - - -
14										- - - - - - - -
15										- - - - - - - -
16										- - - - - - - -
17										- - - - - - - -
18	WDTCON	-	-	-	WDTPS<3:0>				SWDTEN	--- 0 1 0 0 0
19	CMCON0	C2OUT	C1OUT	C2INV	C1INV	CIS	CM<2:0>			0000 0000
1A	PR0	PR0<7:0>								1111 1111
1B	MSCKCON	-	-	-	SLVREN	-	CKMAVG	CKCNTI	-	- - - 0 - 00 -
1C	SOSCPPRL	SOSCPR<7:0>								1111 1111
1D	SOSCPRH	-	-	-	-	SOSCPR<11:8>				---- 1111
1E										- - - - - - - -
1F										- - - - - - - -

Table 16. CMT2189B Special Function Registers Summary Bank1

ADDR	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	POR reset
80	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								x x x x x x x x
81	OPTION	/PAPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111
82	PCL	Program Counter's (PC) Least Significant Byte, PC<7:0>								0000 0000
83	STATUS	-	-	PAGE	/TF	/PF	Z	HC	C	-- 0 1 1 x x x
84	FSR	Indirect Data Memory Address Pointer								
85	TRISA	TRISA<7:6>		--	TRISA<4:0>					11 x 1 1111
86										- - - - - - - -
87	TRISC	TRISC<7:0>								1111 1111
88										- - - - - - - -
89										- - - - - - - -
8A	PCLATH	-	-	-	Write Buffer for upper 5 bits of Program Counter, PC<13:8>					- - - 0 0 0 0 0
8B	INTCON	GIE	PEIE	T0IE	INTE	PAIE	T0IF	INTF	PAIF	0000 0000
8C	PIE1	EEIE	CKMEAIE	-	C2IE	C1IE	OSFIE	TMR2IE	-	00 - 0 0 0 0 -
8D										- - - - - - - -
8E	PCON							/POR	/BOR	- - - - - - q q
8F	OSCCON	LFMOD	IRCF[2:0]			OSTS	HTS	LTS	SCS	0101 x000
90										- - - - - - - -
91										0000 0000
92	PR2	PR2[7:0], Timer2 period register								1111 1111
93										- - - - - - - -
94										- - - - - - - -
95	WPUA	WPUA<7:6>		-	WPUA<4:0>					11 - 1 1111
96	IOCA	IOCA<7:0>								- - - - - - - -
97										- - - - - - - -
98										- - - - - - - -
99	VRCON	VREN	-	VRR	-	VR<3:0>				0 - 0 - 0000
9A	EEDAT	EEDAT<7:0>								0000 0000
9B	EEADR	EEADR<7:0>								0000 0000
9C	EECON1	-	-	WREN3	WREN2	WRERR	WREN1	-	RD	-- 0 0 x 0 - 0
9D	EECON2	-	-	-	-	-	-	-	WR	- - - - - - - 0
9E										- - - - - - - -
9F										- - - - - - - -

6.2 Port A

There have 6 general purpose I/O pins available, PA0~PA4, and PA7, as shown in the table below. Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled, the associated pin may not be used as a general purpose I/O pin.

Table 17. Mapping from the GPIOs to the Pinouts

GPIO	Pinout
PA0	PA0/ICSPCLK
PA1	PA1/ICSPDAT
PA2	PA2
PA3	PA3
PA4	PA4
PA5	×
PA6	×
PA7	PA7/OSC1/CLKI

6.2.1 PORTA and the CPIOA Registers

PORTA is a 6-bit wide, bidirectional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin as input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin as output (i.e., put the contents of the output latch on the selected pin). The exception is PA5, which is input only and its TRISA bit will always read as '1'.

Reading the PORTA register reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read; this value is modified and then written to the PORT data latch. PA5 reads '0' when MCLRE = 1.

6.2.2 Additional Pin Functions

Every PORTA pin on the CMT2189B has an interrupt-on-change(IOC) option and every PORTA pin has a pull-up option.

6.2.2.1 Pull-up

Each of the PORTA pinshas an individually configurable internal pull-up. Control bits WPUA enable or disable each pull-up.

6.2.2.2 Interrupt-On-Change

Each of the PORTA pins is individually configurable as an interrupt-on-change pin. Control bits IOCA enable or disable the interrupt function for each pin. The interrupt-on-change is disabled on a Power-on Reset. For enabled interrupt-on-change pins, the values are compared with the old value latched on the last read of PORTA. The 'mismatch' outputs of the last read are OR'd together to set, the PORTA Change Interrupt Flag bit (PAIF) in the INTCON register. This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, can clear the interrupt by:

1) Any read or write of PORTA. This will end the mismatch condition, then.
2) Clear the flag bit PAIF.

A mismatch condition will continue to set flag bit PAIF. Reading PORTA will end the mismatch condition and allow flag bit PAIF to be cleared. The latch holding the last read value is not affected by a MCLR nor BOD Reset. After these resets, the PAIF flag will continue to be set if a mismatch is present.

6.3 PORTC

PORTC is a general purpose I/O port consisting of 8 bidirectional pins. The pins can be configured for either digital I/O, but only PC4 and PC6 has been pin out. PC0 is connected to the RFDIN, PC1 is connected to the SPI's SDIO, PC2 is connected to the SPI's SCLK, and PC3 is connected to the SPI's CSB, all this four pins are inside in the chip, are not pin out, and are

used to configuration the RF parameters.

Table 18. Mapping from the SPI

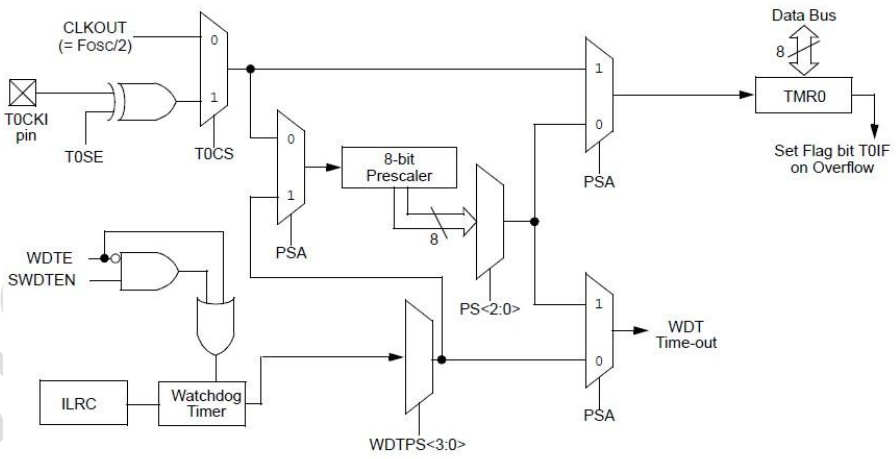
GPIO	RF Part	Pinout
PC0	RFDIN	×
PC1	SDIO	×
PC2	SCLK	×
PC3	CSB	×
PC4	--	PC4
PC5	--	×
PC6	--	PC6
PC7	--	×

6.4 Timer0 Module

The Timer0 module timer/counter has the following features.

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 13 is a block diagram of the Timer0 module and the prescaler shared with the WDT.



Note 1: T0SE, T0CS, PSA, PS<2:0> are bits in the Option register, WDTPS<3:0> are bits in the WDTCON register.

Figure 135. Block Diagram of the Timer0/WDT Prescaler

6.4.1 Timer0 Operation

Timer mode is selected by clearing the T0CS bit(OPTION<5>). In Timer mode, the Timer0module will increment every instruction cycle (without prescaler). If TMR0 is written, the increment is in habited for the following two instruction cycles. The

user can work around this by writing an adjusted value to theTMR0 register.

Counter mode is selected by setting the T0CS bit(OPTION<5>). In this mode, the Timer0 module will increment either on every rising or falling edge of pin PA2/T0CKI. The incrementing edge is determined by the source edge (T0CE) control bit(OPTION<4>). Clearing the T0CE bit selects the rising edge.

6.4.2 Timer0 Interrupt

A Timer0 interrupt is generated when the TMR0register timer/counter overflows from FFh to 00h. This overflow sets the T0IF bit. The interrupt can be masked by clearing the T0IE bit (INTCON<5>). The T0IF bit(INTCON<2>) must be cleared in software by theTimer0 module Interrupt Service Routine before re-enabling this interrupt. The Timer0 interrupt can not wake the processor from Sleep, since the timer is shutoff during Sleep.

6.4.3 Using Timer0 with an External Clock

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI, with the internal phase clocks, is accomplished by sampling the prescaler output on the Q2 andQ4 cycles of the internal phase clocks. Therefore, it is necessary for T0CKI to be high for at least $2T_{OSC}$(and a small RC delay of 20 ns) and low for at least $2T_{OSC}$(and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

6.4.4 Prescaler

An 8-bit counter is available as a prescaler for theTimer0 module, or as a postscaler for the Watchdog Timer. For simplicity, this counter will be referred to as “prescaler” throughout this Datasheet. The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. Prescale values are selectable via the PS2:PS0 bits (OPTION<2:0>). The prescaler is not readable or writable. When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRR 1, STWR 1,BSR 1, x.... etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the Watchdog Timer.

6.5 Timer2 Module

Figure 14 shows the basic block diagram of the Timer2 module.

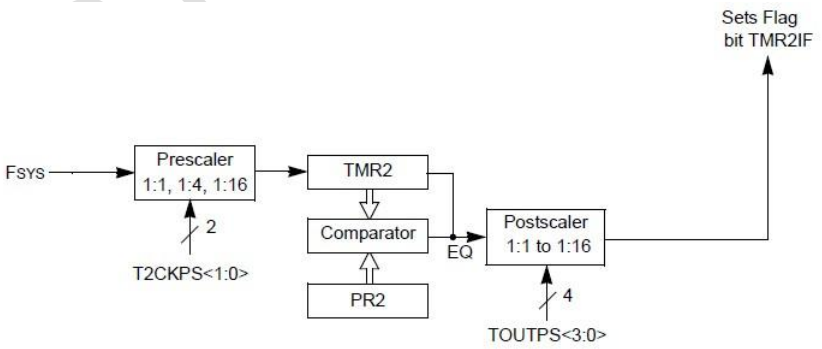


Figure 14. Timer2 Block Diagram

7. Ordering Information

Table 19. CMT2189B Ordering Information

Part Number	Descriptions	Package Type	Package Option	Operating Condition	MOQ / Multiple
CMT2189B-ESR[1]	240 – 960 MHz SoC OOK Transmitter	SOP14	Tape & Reel	2.0 to 3.6 V, -40 to 85 ℃	2,500
CMT2189B-ESB[1]	240 – 960 MHz SoC OOK Transmitter	SOP14	Tube	2.0 to 3.6 V, -40 to 85 ℃	1,000

Notes:

[1]. “E” stands for extended industrial product grade, which supports the temperature range from -40 to +85 ℃.

“S” stands for the package type of SOP14.

“R” stands for the tape and reel package option, the minimum order quantity (MOQ) for this option is 2,500 pcs. “B” stands for the tube package option, with the MOQ of 1,000 pcs.

Visit www.cmostek.com/products to know more about the product and product line.

Contact sales@cmostek.com or your local sales representatives for more information.

8. Package Outline

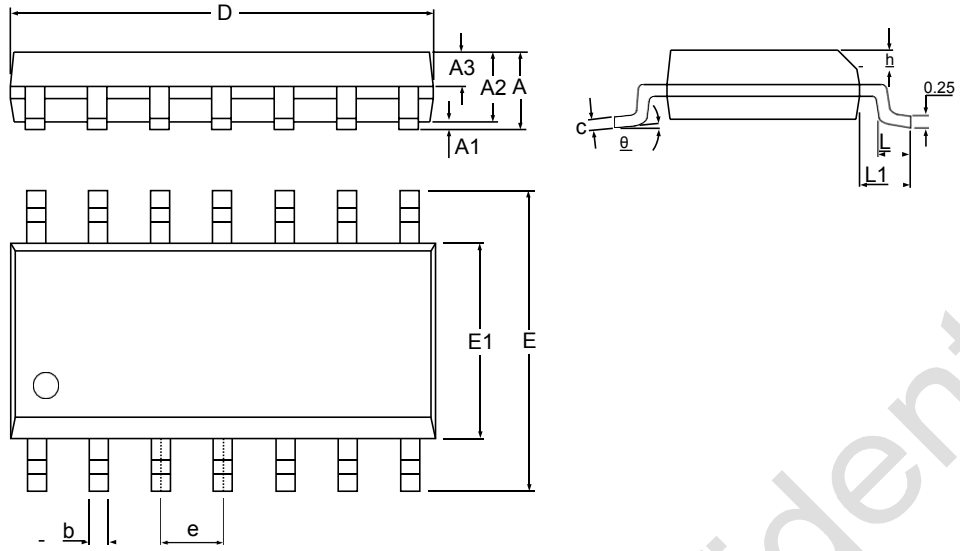


Figure 15.14-Pin SOP Package

Table 20.14-Pin SOP Package Dimensions

Symbol	Size (millimeters)		
	Min	Typ	Max
A	-	-	1.75
A1	0.05	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.48
C	0.21	-	0.26
D	8.45	8.65	8.85
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27 BSC		
h	0.25	-	0.50
L	0.30	-	0.60
L1	1.05 BSC		
θ	0	-	8°

9. Top Marking

9.1 CMT2189B Top Marking

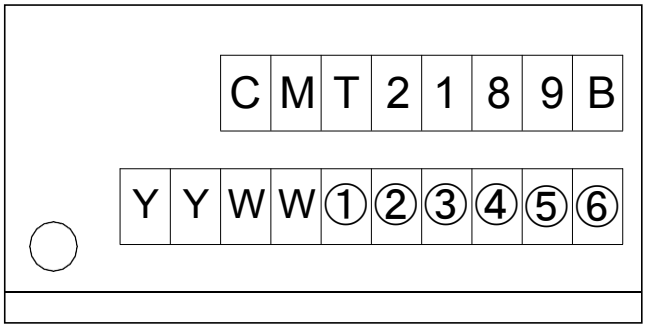


Figure 16. CMT2189B Top Marking

Table 21. CMT2189B Top Marking Explanation

Mark Method :	Laser
Pin 1 Mark :	Circle's diameter = 1 mm.
Font Size :	0.35 mm, right-justified.
Line 1 Marking :	CMT2189B represents part number CMT2189B
Line 2 Marking :	YYWW is the Date code assigned by the assembly house. YY represents the last two digits of the mold year and WW represents the workweek. ①②③④⑤⑥is the internal tracking number.

10. Other Documentations

Table 22. Other Documentations for CMT2189B

Brief	Name	Descriptions
AN159	CMT211xB/CMT215xL_B Transmit Matching Guide(CN)	Details of CMT211xB, CMT215xL & CMT215xB RF matching network and other application layout design related issues.
AN201	CMT2189B User Guide(CN)	Details of using the CMT2189B
AN204	CMT2281F2/CMT2280F2/CMT2189B/CMT2189C IDE Guide(CN)	Details of using the IDE

11. Document Change List

Table 23. Document Change List

Rev. No.	Chapter	Description of Changes	Date
0.5	All	Initial Released	2018-1-1

12. Contact Information

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