HOPERF

CMT2380F29

Ultra-low Power Sub-1GHz Wireless Transceiver

MCU Feature

- A 32-bit ARM Cortex-M0 kernal with single cycle hardware multiply instruction
- 29.5 kB on-chip Flash
  - supports encrypted storage
  - endure more than 100,000 cycles, 10 years of data retention
- 3 kB on-chip SRAM
- Programming method：
  - SWD online debugging interface
- Supports up to 18 multi-functional GPIOs
- Low power management：
  - Run mode: All peripherals are configurable
  - Stop mode: TIM6, IWDG are configurable, SRAM retention, all IO retention
  - Power Down mode（PD）: supports 3 IO wakeup, PA0_NRST, PA1_WKUP0, PA2_WKUP1
- Clock：Up to 48 MHz
  - HSI：Internal high-speed RC OSC 48 MHz / 40 MHz (optional)
  - LSI：Internal low-speed RC OSC 32 kHz
  - MCO: Supports one chanel clock output which can be configured as HSI or LSI post divided output
- Reset
  - Supports power-on/power-down/external pin reset
  - Supports programmable low voltage detection and reset
  - Supports watchdog reset, software reset
- Communication Interface
  - 2 UART interface, support asynchronous mode, multi-processing communication mode, single-wire half-duplex mode
  - 1 SPI interface with rate up to 12MHz
  - 1 I2C interface with rate up to 1MHz, supports master and slave mode configurable
- Analog interface
  - 1x12 bit high-speed ADC, 1 Msps, up to 9 external single-ended input channels, 1 internal channel connected to 1.2V reference
- 1 high speed analog comparator, supports 4 level adjustable voltage 0mV/ 100mV/ 200mV/ 300mV from the positive input end
- A beeper which is output complementarily
- Timer / Counter
  - 1 x 16 bit high speed advance timer counter, supports input capture, comparision output; Each timer has 4 independent channel, of which 3 support 6-channel complementary PWM output
  - 1x16 bit General Timer, 2 independent channels, supports input capture/output comparison/PWM output
  - 1x16 bit Basic Time Counter, supports wakeup low power STOP mode
  - 1x24 bit SysTick
  - 1x12bit independent watchdog (IWDG)
- Security features
  - CRC16 calculation
  - Supports write protection (WRP), multiple read protection (RDP) levels（L0/L1/L2）
- 96 bit UID and 128 bit UCID

RF Features

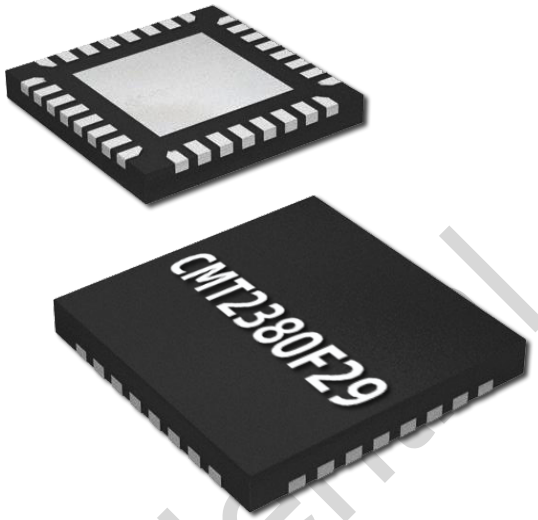
- Working frequency：127 - 1020 MHz
- Modulation style： (G)FSK，(G)MSK，OOK
- Data rate： 0.5 - 300 kbps
- Sensitivity： -121 dBm @ 434 MHz，FSK
- RX current： 8.5 mA @ 434 MHz，FSK
- TX current： 72 mA @ 20 dBm, 434 MHz
- Maximum configurable FIFO of 64 Byte

System Features

- Working voltage：2.0 ~ 3.6 V
- Working temperature：-40 ~ +85℃
- ESD: ±2KV（HBM model）,
  ±1KV（CDM model）
- QFN32 5x5 package

Overview

CMT2380F29 integrates a 32-bit ARM Cortex®-M0 core with a super low power consumption RF transceiver. It is a high efficiency super-low power MCU, applying for wireless application of (G) FSK、(G) MSK and OOK transceiver from 127 to 1020 MHz. CMT2380F29 operates from 2.0 V to 3.6 V and supports up to +20 dBm TX power consumption and -121 dBm receiving sensitivity with the corresponding TX current and RX current of 72 mA and 8.5 mA.(MCU power consumption is not included). CMT2380F29 integrates a wealth of peripherals supports standard UART, I2C and SPI interface, with up to 18 general IO, supports internal high speed /low speed low power consumption RC oscillator and 32.768 kHz external crystal oscillator, supports a variety of packet formats and encoding and decoding methods up to 64-byte Tx/Rx FIFO, supports featured rich RF GPIO, a variety of low power operation mode and fast startup mechanism, high precision RSSI, manual fast frequency hopping and 12 bit high speed ADC multi-channel input,etc. CMT2380F29 has a small QFN package size of 5mmx5mm, which is ideal for small size and power consumption of Internet applications.



Application

- Auto metering
- Home security and building automation
- Wireless sensor nodes and industrial monitoring
- ISM band data communication

Table 1. CMT2380F29 Resources List

Memory		Analog peripheral		Digital peripheral						
ROM	RAM	ADC	PDR	RTC	WDT	Timer	UART	SPI	I2C	GPIO
29.5KB Flash	3KB	12bits x 9-ch 1Msps	√	1	1	5	2xUSART	1	1	18

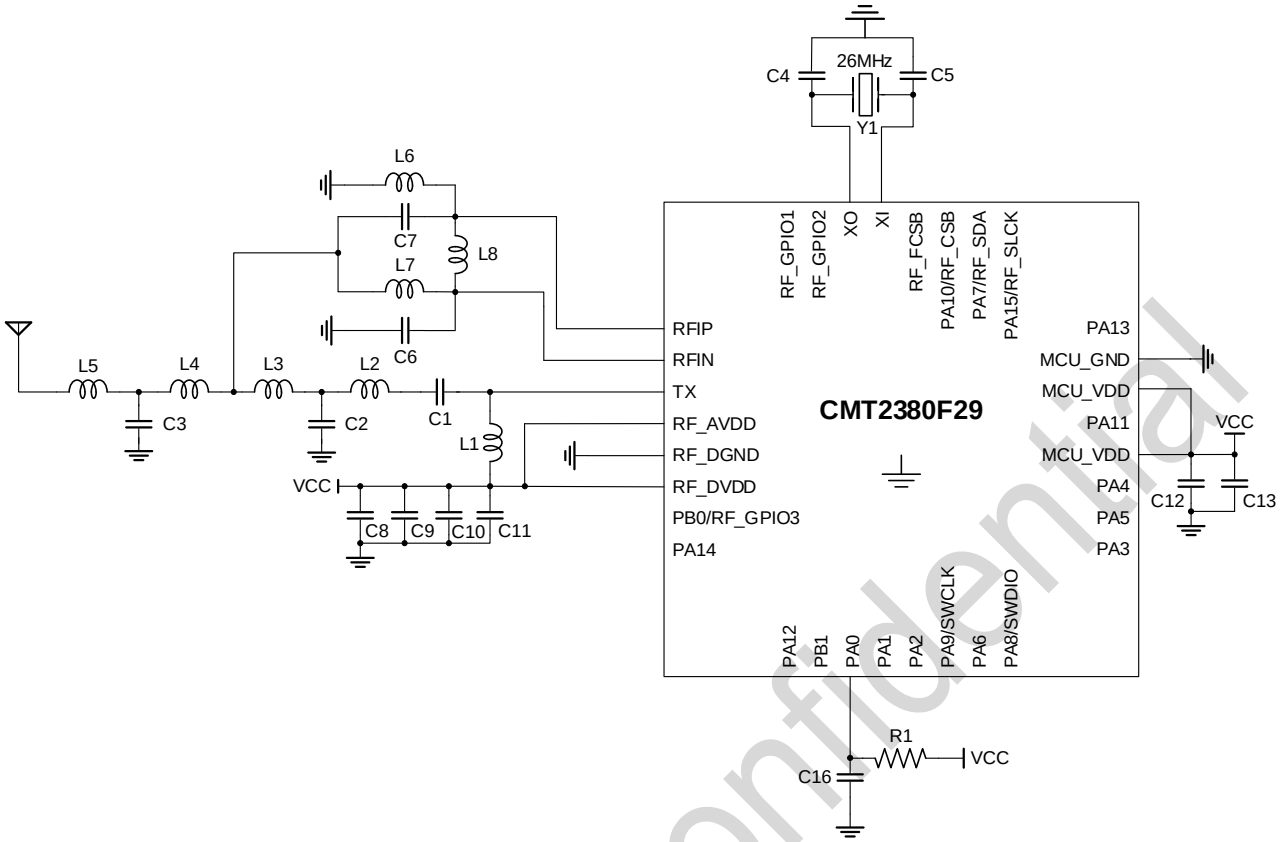


Figure 2. CMT2380F29（QFN32 5x5）Typical Application Diagram（20 dBm power output）

No.	Description	Component value			Unit	Supplier
		434 MHz	868 MHz	915 MHz		
C1	±5%, 0402 NP0, 50 V	15	18	18	pF	-
C2	±5%, 0402 NP0, 50 V	3	3.6	3.6	pF	-
C3	±5%, 0402 NP0, 50 V	6.2	3.3	3.3	pF	-
C4	±5%, 0402 NP0, 50 V	24	24	24	pF	-
C5	±5%, 0402 NP0, 50 V	24	24	24	pF	-
C6	±5%, 0402 NP0, 50 V	4.7	2	1.8	pF	-
C7	±5%, 0402 NP0, 50 V	4.7	2	1.8	pF	-
C8	±20%, 0603 X7R, 25 V	4.7			uF	-
C9	±5%, 0402 NP0, 50 V	470			pF	-
C10	±20%, 0402 X7R, 25 V	0.1			uF	
C11	±20%, 0402 X7R, 25 V	0.1			uF	
C12	±20%, 0402 X7R, 25 V	0.1			uF	-
C13	±20%, 0603 X7R, 25 V	1			uF	-
C14	±20%, 0402 X7R, 25 V	0.1			uF	-

No.	Description	Component value			Unit	Supplier
		434 MHz	868 MHz	915 MHz		
C15	±20%, 0603X7R, 25 V	1			uF	-
C16	±20%, 0402 X7R, 25 V	0.1			uF	
R1	±5%, 0603 Chip Resistor	10			kΩ	
L1	±10%, 0603 Multi-layer Chip Inductor	180	100	100	nH	Sunlord SDCL
L2	±10%, 0603 Multi-layer Chip Inductor	22	12	12	nH	Sunlord SDCL
L3	±10%, 0603 Multi-layer Chip Inductor	15pF	15	15	nH	Sunlord SDCL
L4	±10%, 0603 Multi-layer Chip Inductor	33	6.2	6.2	nH	Sunlord SDCL
L5	±10%, 0603 Multi-layer Chip Inductor	33	6.2	6.2	nH	Sunlord SDCL
L6	±10%, 0603 Multi-layer Chip Inductor	27	15	15	nH	Sunlord SDCL
L7	±10%, 0603 Multi-layer Chip Inductor	27	15	15	nH	Sunlord SDCL
L8	±10%, 0603 Multi-layer Chip Inductor	68	12	12	nH	Sunlord SDCL
Y1	±10 ppm, SMD32*25 mm	26			MHz	
U1	CMT2380F29, Ultra low power consumption Sub-1 GHz Wireless transceiver single chip	-			-	CMOSTEK

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1 Electrical Characteristic

VDD= 3.3 V，TOP= 25 ° C，FRF = 433.92 MHz, sensitivity is measured by receiving a PN9 coded data and matching impedance to 50Ω under 0.1% BER standard.Unless otherwise stated, all results are tested on the CMT2380F29-EB evaluation board.

1.1 Recommended Operation Condition

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating power voltage	VDD	CPU Working rate 0-48MHz	2.0		3.6	V
	VDD	Part of the analog working voltage while using ADC and COMP	2.4		3.6	V
Operating temperature	TOP		-40		85	℃
Voltage slope	VPSR	VDD rising rate，from 0 to VDD	20			us/V
	VPFR	VDD falling rate，from 0 to VDD	50			us/V
AHB clock frequency	fHCLK		0		48	MHz
APB1 clock frequency	fPCLK1		0		48	MHz

1.2 Absolute Maximum Rating

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}		-0.3	3.6	V
Interface Voltage	V_{IN}		-0.3	3.6	V
Junction Temperature	T_J		-40	125	℃
Storage Temperature	T_{STG}		-50	150	℃
Soldering Temperature	T_{SDR}	Retention at least 30 s		255	℃
ESD Rating[2]		Human body mode (HBM)	-2	2	kV
Latch-up Current		@ 85 ℃	-100	100	mA
MCU-VDD maximum current to Ground				200	mA
MCU pin maximum sink current				16	mA

Notes：

[1]. Exceeding the Absolute Maximum Ratings may cause permanent damage to the equipment. This value is a pressure rating and does not imply that the function of the equipment is affected under this pressure condition, but if it is exposed to absolute maximum ratings for extended periods of time, it may affect equipment reliability.

[2]. CMT2380F29 is a high performance RF integrated circuit. The operation and assembly of this chip should only be performed on a workbench with good protection.

Caution! ESD sensitive device. Precaution should be made when handling the device in order to prevent permanent damage.

1.3 Power Consumption

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Sleep current	I_{SLEEP}	Sleep mode, sleep timer is off		300		nA
		Sleep mode, sleep timer is on		800		nA
Standby current	$I_{Standby}$	晶体振荡器开启		1.45		mA
RFS current	I_{RFS}	433 MHz		5.7		mA
		868 MHz		5.8		mA
		915 MHz		5.8		mA
TFS current	I_{TFS}	433 MHz		5.6		mA
		868 MHz		5.9		mA
		915 MHz		5.9		mA
RX current (high performance)	I_{Rx-HP}	FSK, 433 MHz, 10 kbps,10 kHz F_{DEV}		8.5		mA
		FSK, 868 MHz, 10 kbps, 10 kHz F_{DEV}		8.6		mA
		FSK, 915 MHz, 10 kbps,10 kHz F_{DEV}		8.9		mA
RX current (low power consumption)	I_{Rx-LP}	FSK, 433 MHz, 10 kbps, 10 kHz F_{DEV}		7.2		mA
		FSK, 868 MHz, 10 kbps, 10 kHz F_{DEV}		7.3		mA
		FSK, 915 MHz, 10 kbps, 10 kHz F_{DEV}		7.6		mA
TX current	I_{Tx}	FSK, 433 MHz, +20 dBm (Direct)		72		mA
		FSK, 433 MHz, +20 dBm (RF switch)		77		mA
		FSK, 433 MHz, +13 dBm (Direct)		23		mA
		FSK, 433 MHz, +10 dBm (Direct)		18		mA
		FSK, 433 MHz, -10 dBm (Direct)		8		mA
		FSK, 868 MHz, +20 dBm (Direct)		87		mA
		FSK, 868 MHz, +20 dBm (RF switch)		80		mA
		FSK, 868 MHz, +13 dBm (Direct)		27		mA
		FSK, 868 MHz, +10 dBm (Direct)		19		mA
		FSK, 868 MHz, -10 dBm (Direct)		8		mA
		FSK, 915 MHz, +20 dBm (Direct)		70		mA
		FSK, 915 MHz, +20 dBm (RF switch)		75		mA
		FSK, 915 MHz, +13 dBm (Direct)		28		mA
		FSK, 915 MHz, +10 dBm (Direct)		19		mA
		FSK, 915 MHz, -10 dBm (Direct)		8		mA

Notes: The above power consumption is only RF working current, excluding the working current of the controller part.

1.4 RF Receiver Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Data rate	DR	OOK	0.5		40	kbps
		FSK 和 GFSK	0.5		300	kbps
Deviation	F_{DEV}	FSK 和 GFSK	2		200	kHz
Sensitivity @ 433 MHz	$S_{433\text{-}HP}$	DR = 2.0 kbps, F_{DEV} = 10 kHz		-121		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz		-116		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz (Low power setting)		-115		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz		-113		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz (Low power setting)		-112		dBm
		DR = 50 kbps, F_{DEV} = 25 kHz		-111		dBm
		DR =100 kbps, F_{DEV} = 50 kHz		-108		dBm
		DR =200 kbps, F_{DEV} = 100 kHz		-105		dBm
		DR =300 kbps, F_{DEV} = 100 kHz		--103		dBm
Sensitivity @ 868 MHz	$S_{868\text{-}HP}$	DR = 2.0 kbps, F_{DEV} = 10 kHz		-119		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz		-113		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz (Low power setting)		-111		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz		-111		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz (Low power setting)		-109		dBm
		DR = 50 kbps, F_{DEV} = 25 kHz		-108		dBm
		DR =100 kbps, F_{DEV} = 50 kHz		-105		dBm
		DR =200 kbps, F_{DEV} = 100 kHz		-102		dBm
		DR =300 kbps, F_{DEV} = 100 kHz		-99		dBm
Sensitivity @ 915 MHz	$S_{915\text{-}HP}$	DR = 2.0 kbps, F_{DEV} = 10 kHz		-117		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz		-113		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz (Low power setting)		-111		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz		-111		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz (Low power setting)		-109		dBm
		DR = 50 kbps, F_{DEV} = 25 kHz		-109		dBm
		DR =100 kbps, F_{DEV} = 50 kHz		-105		dBm
		DR =200 kbps, F_{DEV} = 100 kHz		-102		dBm
		DR =300 kbps, F_{DEV} = 100 kHz		--99		dBm
Saturation Input Signal Level	P_{LVL}				20	dBm
Image Rejection Ratio	IMR	F_{RF}=433 MHz		35		dB
		F_{RF}=868 MHz		33		dB
		F_{RF}=915 MHz		33		dB
RX Channel Bandwidth	BW	RX channel bandwidth	50		500	kHz
Co-channel Rejection Ratio	CCR	DR = 10 kbps, F_{DEV} = 10 kHz; Interfere with the same modulation		-7		dB

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Adjacent Channel Rejection Ratio	ACR-I	DR = 10 kbps, F_{DEV} = 10 kHz; BW=100kHz, 200 kHz Channel spacing, interfere with the same modulation		30		dB
Alternate Channel Rejection Ratio	ACR-II	DR = 10 kbps, F_{DEV} = 10 kHz; BW=100kHz, 400 kHz Channel spacing, interfere with the same modulation		45		dB
Blocking Rejection Ratio	BI	DR = 10 kbps, F_{DEV} = 10 kHz; ±1 MHz Deviation, continuous wave interference		70		dB
		DR = 10 kbps, F_{DEV} = 10 kHz; ± 2 MHz Deviation, continuous wave interference		72		dB
		DR = 10 kbps, F_{DEV} = 10 kHz; ±10 MHz Deviation, continuous wave interference		75		dB
Input 3rd Order Intercept Point	IIP3	DR = 10 kbps, F_{DEV} = 10 kHz; 1 MHz and 2 MHz Deviation dual tone test, maximum system gain setting		-25		dBm
RSSI Range	RSSI		-120		20	dBm
More Sensitivity (Typical Configuration)		433.92 MHz, DR = 1.2kbps, F_{DEV} = 5 kHz		-122.9		dBm
		433.92 MHz, DR = 1.2kbps, F_{DEV} = 10 kHz		-121.8		dBm
		433.92 MHz, DR = 1.2kbps, F_{DEV} = 20 kHz		-119.5		dBm
		433.92 MHz, DR = 2.4kbps, F_{DEV} = 5 kHz		-120.6		dBm
		433.92 MHz, DR = 2.4kbps, F_{DEV} = 10 kHz		-120.3		dBm
		433.92 MHz, DR = 2.4kbps, F_{DEV} = 20 kHz		-119.7		dBm
		433.92 MHz, DR = 9.6 kbps, F_{DEV} = 9.6 kHz		-116.0		dBm
		433.92 MHz, DR = 9.6 kbps, FDEV = 19.2 kHz		-116.1		dBm
		433.92 MHz, DR = 20 kbps, FDEV = 10 kHz		-114.2		dBm
		433.92 MHz, DR = 20 kbps, FDEV = 20 kHz		-113.0		dBm
		433.92 MHz, DR = 50 kbps, FDEV = 25 kHz		-110.6		dBm
		433.92 MHz, DR = 50 kbps, FDEV = 50 kHz		-109.0		dBm
		433.92 MHz, DR = 100 kbps, FDEV = 50 kHz		-107.8		dBm
		433.92 MHz, DR = 200 kbps, FDEV = 50 kHz		-103.5		dBm
		433.92 MHz, DR = 200 kbps, FDEV = 100 kHz		-104.3		dBm
		433.92 MHz, DR = 300 kbps, FDEV = 50 kHz		-98.0		dBm
		433.92 MHz, DR = 300 kbps, FDEV = 150 kHz		-101.6		dBm

1.5 RF Transmitter Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output power	P_{OUT}	Specific peripheral materials are needed for different frequency bands	-20		+20	dBm
Output power step	P_{STEP}			1		dB
GFSK Gaussian filter coefficient	BT		0.3	0.5	1.0	-
Output power variation	$P_{OUT-TOP}$	Temperature from -40 to +85℃		1		dB
Transmitting spurious emission		P_{OUT} = +13 dBm,433MHz, F_{RF}<1 GHz			-54	dBm
		1 GHz to 12.75 GHz，with harmonic			-36	dBm
Harmonic output for F_{RF}= 433 MHz [1]	$H2_{433}$	2nd harmonic +20 dBm P_{OUT}		-46		dBm
	$H3_{433}$	3rd harmonic +20 dBm P_{OUT}		-50		dBm
Harmonic output for F_{RF}= 868 MHz[1]	$H2_{868}$	2nd harmonic +20 dBm P_{OUT}		-43		dBm
	$H3_{868}$	3nd harmonic +20 dBm P_{OUT}		-52		dBm
Harmonic output for F_{RF}= 915 MHz[1]	$H2_{915}$	2nd harmonic +20 dBm P_{OUT}		-48		dBm
	$H3_{915}$	3nd harmonic +20 dBm P_{OUT}		-53		dBm
Harmonic output for F_{RF}= 433 MHz[1]	$H2_{433}$	2nd harmonic +13 dBm P_{OUT}		-52		dBm
	$H3_{433}$	3nd harmonic +13 dBm P_{OUT}		-52		dBm
Harmonic output for F_{RF}= 868 MHz[1]	$H2_{868}$	2nd harmonic +13 dBm P_{OUT}		-52		dBm
	$H3_{868}$	3nd harmonic +13 dBm P_{OUT}		-52		dBm
Harmonic output for F_{RF}= 915 MHz[1]	$H2_{915}$	2nd harmonic +13 dBm P_{OUT}		-52		dBm
	$H3_{915}$	3nd harmonic +13 dBm P_{OUT}		-52		dBm

Notes:

The harmonic parameter values depend on the quality of the hardware matching network. The above data is measured based on the CMT2380F29-EB module; testing results will be differently when it is done on the self-designed PCB.

1.6 Settling Time of RF Status Switching

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Settling time	T_{SLP-RX}	From Sleep to RX		1000		us
	T_{SLP-TX}	From Sleep toTX		1000		us
	T_{STB-RX}	From Standby to RX		350		us
	T_{STB-TX}	From Standby toTX		350		us
	T_{RFS-RX}	From RFS to RX		20		us
	T_{TFS-RX}	From TFS toTX		20		us
	T_{TX-RX}	From TX to RX （Ramp Down time needs 2 T_{symbol}）		2 T_{symbol} +350		us
	T_{RX-TX}	From RX to TX		350		us

Notes:

[1]. Both of T_{SLP-RX} and T_{SLP-TX} are depend on the crystal oscillator startup time, which is mainly related to the crystal itself.

1.7 RF Frequency Synthesizer

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	F_{RF}	Different matching network is required	760		1020	MHz
			380		510	MHz
			190		340	MHz
			127		170	MHz
Synthesizer frequency resolution	F_{RES}			25		Hz
Frequency tuning time	t^{TUNE}			150		us
Phase noise@ 433 MHz	PN_{433}	10 kHz frequency deviation		-94		dBc/Hz
		100 kHz frequency deviation		-99		dBc/Hz
		500 kHz frequency deviation		-118		dBc/Hz
		1 MHz frequency deviation		-127		dBc/Hz
		10 MHz frequency deviation		-134		dBc/Hz
Phase noise@ 868 MHz	PN_{868}	10 kHz frequency deviation		-92		dBc/Hz
		100 kHz frequency deviation		-95		dBc/Hz
		500 kHz frequency deviation		-114		dBc/Hz
		1 MHz frequency deviation		-121		dBc/Hz
		10 MHz frequency deviation		-130		dBc/Hz
Phase noise@ 915 MHz	PN_{915}	10 kHz frequency deviation		-89		dBc/Hz
		100 kHz frequency deviation		-92		dBc/Hz
		500 kHz frequency deviation		-111		dBc/Hz
		1 MHz frequency deviation		-121		dBc/Hz
		10 MHz frequency deviation		-130		dBc/Hz

1.8 Crystal Oscillator Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal frequency[1]	F_{XTAL}			26		MHz
Frequency tolerance[2]	ppm			20		ppm
Load capacitance	C_{LOAD}			15		pF
Equivalentresistance	Rm			60		Ω
Start-up time[3]	t^{XTAL}			400		us

Notes:

[1]. CMT2380F29 can use the external reference clock to drive the XIN pin through the coupling capacitor. The peak value of the external clock signal is between 0.3 V and 0.7 V.

[2]. The value includes (1) initial error; (2) crystal load; (3) aging; and (4) change with temperature. The acceptable crystal frequency tolerance is limited by the receiver bandwidth and the RF frequency offset between the transmitter and the receiver.

[3]. The parameter is largely related to the crystal.

1.9 Controller Reset and Power Control Module Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
V_{PVD}	Rising	PVD[3:0]=0	1.8	1.88	1.96	V
	Falling	PVD[3:0]=0	1.7	1.78	1.86	
	Rising	PVD[3:0]=1	2	2.08	2.16	
	Falling	PVD[3:0]=1	1.9	1.98	2.06	
	Rising	PVD[3:0]=2	2.2	2.28	2.36	
	Falling	PVD[3:0]=2	2.1	2.18	2.26	
	Rising	PVD[3:0]=3	2.4	2.48	2.56	
	Falling	PVD[3:0]=3	2.3	2.38	2.46	
	Rising	PVD[3:0]=4	2.6	2.68	2.76	
	Falling	PVD[3:0]=4	2.5	2.58	2.66	
	Rising	PVD[3:0]=5	2.8	2.88	2.96	
	Falling	PVD[3:0]=5	2.7	2.78	2.86	
	Rising	PVD[3:0]=6	3	3.08	3.16	
	Falling	PVD[3:0]=6	2.9	2.98	3.06	
	Rising	PVD[3:0]=7	3.2	3.28	3.36	
	Falling	PVD[3:0]=7	3.1	3.18	3.26	
	Rising	PVD[3:0]=8	3.4	3.48	3.56	
	Falling	PVD[3:0]=8	3.3	3.38	3.46	
	Reserve	other	--	--	--	
$V_{PVDhyst}$(1)	PVD Hysterisis	-	80	100	125	mV
V_{LVR}	Rising	LVR[3:0]=0	1.8	1.88	1.96	V
	Falling	LVR[3:0]=0	1.7	1.78	1.86	V
	Rising	LVR[3:0]=1	2	2.08	2.16	
	Falling	LVR[3:0]=1	1.9	1.98	2.06	
	Rising	LVR[3:0]=2	2.2	2.28	2.36	
	Falling	LVR[3:0]=2	2.1	2.18	2.26	
	Rising	LVR[3:0]=3	2.4	2.48	2.56	
	Falling	LVR[3:0]=3	2.3	2.38	2.46	
	Rising	LVR[3:0]=4	2.6	2.68	2.76	
	Falling	LVR[3:0]=4	2.5	2.58	2.66	
	Rising	LVR[3:0]=5	2.8	2.88	2.96	
	Falling	LVR[3:0]=5	2.7	2.78	2.86	
	Rising	LVR[3:0]=6	3	3.08	3.16	
	Falling	LVR[3:0]=6	2.9	2.98	3.06	
	Rising	LVR[3:0]=7	3.2	3.28	3.36	
	Falling	LVR[3:0]=7	3.1	3.18	3.26	
	Rising	LVR[3:0]=8	3.4	3.48	3.56	
	Falling	LVR[3:0]=8	3.3	3.38	3.46	
	Reserve	other	--	--	--	
$V_{LVRhyst}$(1)	LVR hysterisis	--	80	100	125	mV
$V_{POR/PDR}$	VDD power up/ down reset threshold value	--	--	1.53	--	V
$T_{RSTTEMPO}$(1)	Reset duration time	--	--	150	--	μs

1. Values are guaranteed by designed, not tested in production.

1.10 Controller Embedded Reference Voltage

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Embedded reference voltage	V_{REFINT}	-40℃< TA< +85℃	-	1.21	-	V
Sampling time of ADC	$T_{S\_vrefint}$(1)	PLS[3:0]=0001 (rising edge), f_{ADC_CLK}=24M	-	15.8	-	μs

when internal reference voltage read out						
1. The minimum sampling time was obtained from multiple cycles in application.						

1.11 Controller Working Current Characteristic

Current consumption is made up of several parameters and factors, including operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin turnover rate, program location in memory, and code executed, etc.

- Maximum current consumption

The micro-controller is under the following conditions：

- All I / O pins are in input mode and are connected to a static level V_{DD} or V_{SS} with no load.
- All peripherals are disabled, unless otherwise noted.
- The access time of the flash memory is adjusted to the f_{HCLK} frequency (0 wait period for 0 to 24 MHz, 1 wait period for 24 to 48 MHz).
- The command pre-fetch function is turned on (notes: this parameter must be set before the clock and bus frequency distribution is set).
- When the peripherals are turned on：$f_{PCLK1} = f_{HCLK}$.

Table 1-11-1. Maximum Current Consumption in Operating Mode and Data Processing Code Run from the Internal Flash Memory

Sign	Parameter	Condition	f_{HCLK}	Typical value(1)	Unit
				T_A = 85℃	
I_{DD}	Operating current in operating mode	Internal clock, enable all the peripherals	48MHz	4.92	mA
			40MHz	4.03	
			24MHz	3.0	
			8MHz	2.01	
		Internal clock, disable all the peripherals	48MHz	4.0	
			40MHz	3.3	
			24MHz	2.51	
			8MHz	1.8	
1. Guaranteed by design and comprehensive assessment, not tested in production.					

- **Typical current consumption**

MCU is under conditions as followed：

- All I / O pins are in input mode and are connected to a static level VDD or VSS with no load.
- All peripherals are disabled, unless otherwise noted.
- The access time of the flash memory is adjusted to the f_{HCLK} frequency (0 wait period for 0 to 24 MHz, 1 wait period for 24 to 48 MHz).
- The command pre-fetch function is turned on (notes: this parameter must be set before the clock and bus frequency distribution is set).
- When the peripherals are turned on：$f_{PCLK} = f_{HCLK}$，$f_{ADCCLK} = f_{PCLK}/2$

- Low current consumption

MCU is under conditions as followed

- All I / O pins are in input mode and are connected to a static level VDD or VSS with no load.
- All peripherals are disabled, unless otherwise noted.

Table 1-11-2. Typical Consumption in Stop and Sleep Mode

Parameter	Symbol	Condition	Typ (1)	Max(1)	Unit
			VDD=3.3V		
I_{DD_STOP}	STOP mode current	LSI=32KHz, HCLK is off，3KB SRAM, registers and all I/O retain	2	-	μA
I_{DD_PD}	PD mode current	All function module off and support 2 channel WAKEUP IO	0.5	-	μA
1 Typ/ Max value is tested under TA=25 ℃.					

1.12 Controller Internal Clock Source Characteristics

- High speed internal (HIS) RC Oscillator

Table1-12-1. HSI Oscillator Characteristic(1)(2)

Sign	Parameter	Condition	Min	Typ	Max	Unit
f_{HSI}	Frequency	HSI=48M，VDD=3.3V，T_A = 25℃，after calibration	47.52(3)	48	48.48(3)	MHz
		HSI=40M，VDD=3.3V，T_A = 25℃，after calibration	39.6(3)	40	40.4(3)	MHz
$DuCy_{(HSI)}$	Duty cycle	-	45	-	55	%
ACC_{HSI}	HSI oscillator temperature drift(4)	VDD=3.3V，T_A = -40~85 ℃，temperature drift	-2	-	2.7	%
		VDD=3.3V，T_A = -20~85℃，temperature drift	-1.5	-	2.7	%
		VDD=3.3V，T_A = 0~70℃，temperature drift	-1	-	2	%
$t_{SU(HSI)}$	HSI oscillator startup time		2	-	7	μs
$I_{DD(HSI)}$	HSI oscillator power consumption		-	250	400	μA

1. Unless otherwise specified, VDD = 3.3V，TA = -40~85℃.
2. Guaranteed by design and comprehensive assessment, not tested in production.
3. The production accuracy is not influenced by welding. The frequency deviation by welding is at the range of ±1%.
4. Frequency deviation includes the effect of welding is from sample testing, not from testing in production.

- Internal Low-speed Oscillator (LSI)RC

Table1-12-2.LSI Oscillator Characteristic(1)

Sign	Parameter	Condition	Min	Typ	Max	Unit
f_{LSI}(2)	Output frequency	25℃ calibration, VDD = 3.3V	31	32	33	KHz
		VDD =2.0V ~ 3.6V,TA = -40 ~ 85℃	26	32	38	KHz
$t_{SU(LSI)}$ (2)	LSI Oscillator starup time	-	-	30	80	μs
$I_{DD(LSI)}$ (2)	LSI power consumption	-	-	0.3	-	μA

1. Unless otherwise specified, VDD = 3.3V，TA = -40~85℃.
2. Guaranteed by design and comprehensive assessment, not tested in production.

1.13 Controller Low-Power Mode Wake-Up Time

The arousal times listed in the table below are measured during the arousal phase of an 48MHz HIS RC oscillator. The clock source used on wake-up depends on the current mode of operation:

- Stop or Sleep mode：the clock source is RC oscillator

Table1-13-1. Wake-up Time in the Low-Power Mode

Symbol	Parameter	Typ	Unit
t_{WUSTOP}(1)	Awaken from stop mode	22	μs
t_{WUPD}(1)	Awaken from stanby mode	560	μs

1. The awaken time counts from the beginning of the wake up event until the user program reads the first instruction;

1.14 Controller Flash Characteristic

Table1-14-1. FLASH Characteristics

Sign	Parameter	Condition	Min	Typ	Max	Unit
t_{prog}	Word programming time(32-bit)	T_A = -40~85℃	-	175	-	μs
t_{ERASE}	Page erase time (512 Bytes)	T_A = -40~85℃	-	2.27	-	ms
t_{ME}	Mass erase time	TA = -40~85℃；BOOT UNLOCK	-	70.6	-	ms

		TA = -40~85℃； BOOT LOCK		132.8		
IDD	Supply current (1)	Read，fHCLK=48MHz，，VDD=3.3V	-	2	2.4	mA
		Write，fHCLK=48MHz，VDD=3.3V	-	-	1.2	mA
		Erase，fHCLK=48MHz，VDD=3.3V	-	-	0.6	mA
		PD mode, VDD=3.3~3.6V	-	-	150	μA
1. Guaranteed by design and comprehensive evaluation, not tested in production.						

Table 1-14-2. Flash Memory Life and Data Retention Period

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance (Note: erasing and writing cycle)	TA = -40~85°C；	100	kcycles
t_{RET}	Data retention	TA = 85°C，after 1000 erasing and cycle	10	years
1. Guaranteed by design and comprehensive evaluation, not tested in production.				

1.15 Absolute Maximum Rating（Electrical Sensitivity）

Strength test is done of the chip to determine its performance in electrical charachteristic in 3 different test methods (ESD, LU) specifically.

■ **Electrostatic discharge（ESD）**

Electrostatic discharge (a positive pulse followed by a negative pulse one second later) is applied to all pins of all samples.

Table 1-15-1. ESD Characteristics

Symbol	Parameter	Conditions	Class	Max(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = +25 °C， complies with MIL-STD-883K Method 3015.9	2	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charging equipment model)	T_A = +25 °C，complies with ESDA/JEDEC JS-002-2018	II	1000	
1. Guaranteed by design and comprehensive evaluation, not tested in production.					

■ **Static latchup（LU）**

Two complementary static latchup tests of six samples are required to test the latchup perfprmance.

- Supply voltage exceeding the limit of each power supply pin.
- Current is input into each I/O pin which is used for input, output, and configurable.

This test complies with the EIA/JESD78E integrated circuit latch standard.

Table 1-15-2. Static Latchup Feature

Symbol	Parameter	Conditions	Class
LU	Static latchup	T_A = +85 °C， complies with JESD78E standard	II class A

1.16 Controller IO Port Characteristic

● Generic input/output characteristics

All of the I/O ports are compatible with CMOS and TTL.

Table 1-16-1. I/O Static Characteristics

Symbol	Parameter	VDD	Conditions	Min	Max	Unit
V_{IL}	Low level input voltage	5.0	--	--	0.3×VDD	V
		3.3	--	--	0.8	
		2.0	--	--	0.2×VDD	
V_{IH}	High level input voltage	5.0	--	0.7×VDD	--	
		3.3	--	2.0	--	
		2.0	--	0.8×VDD	--	
V_{hys}	I/O Schmitt trigger voltage Hysteresis (1)	3.3/2.0	--	0.1×VDD	--	V
I_{lkg}(2)	Input leakage current I_{IH}	3.3/2.0	--	--	1	μA
	Input leakage current I_{IL}	3.3/2.0	--	-1	--	
	Output high level voltage	3.3	High driving Imin=8mA low driving Imin=4mA	2.4	--	
		2.0	High driving Imin=4mA low driving Imin=2mA	VDD-0.45	--	
V_{OL}	Output low level voltage	3.3	High driving Imin=8mA low driving Imin=4mA	-	0.45	V
		2.0	High driving Imin=4mA low driving Imin=2mA	-	0.4	
R_{PU}	Internal pull-up resistor	3.3/2.0	-	20	100	kΩ
R_{PD}	Internal pull-down resistor	3.3/2.0	-	20	100	kΩ
C_{IO}	I/O pin capacitance	3.3/2.0	-	-	10	pF

1. Guaranteed by design and comprehensive evaluation, not tested in production.

2. If there is reverse current in the adjacent pin, the leakage current may be higher than the maximum value.

All I/O ports are CMOS and TTL compatible (no software configuration required) and their features take most of the strict CMOS process or TTL parameters into account.

● Input and output AC characteristics

The parameters and definition of I/O AC are shown as followed.

Table 1-16-2. I/O AC Characteristics

VDD	Condition			Rise/Fall Time (ns)			Propagation Delay (ns)		
	Driving Strength	Slew Rate Control	Cloading (pf)	Min	Typ	Max	Min	Typ	Max
3.3V(2.7~3.6)	Low (DR=1)	Slow (SR=1)	25	3.32	5.02	9.31	4.74	7.32	13.6
			50	6.06	9.23	17.4	6.27	9.57	17.7
			100	11.7	17.9	33.6	9.31	14	25.8
		Fast (SR=0)	25	3.06	4.67	8.79	4.17	6.52	12.2
			50	5.91	9.02	17	5.69	8.75	16.2
			100	11.7	17.8	33.5	8.73	13.2	24.3
	High (DR=0)	Slow (SR=1)	25	2.08	3.16	5.84	3.93	6.12	11.4
			50	3.34	5.05	9.27	4.72	7.3	13.6
			100	5.97	9.16	17.2	6.25	9.54	17.6
		Fast (SR=0)	25	1.75	2.66	4.91	3.41	5.41	10.2
			50	3	4.62	8.67	4.16	6.51	12.2
			100	5.87	8.92	16.8	5.66	8.72	16.2
1.8V(1.6~2.0)	Low (DR=1)	Slow (SR=1)	25	6.08	10.2	18.1	8.41	14.5	26.6
			50	11	18.4	32.9	11	18.9	34.5
			100	21	35	64	16.3	27.6	49.5
		Fast (SR=0)	25	5.58	9.34	16.7	7.38	12.8	23.7
			50	10.6	17.7	32.3	9.98	17.2	31.6

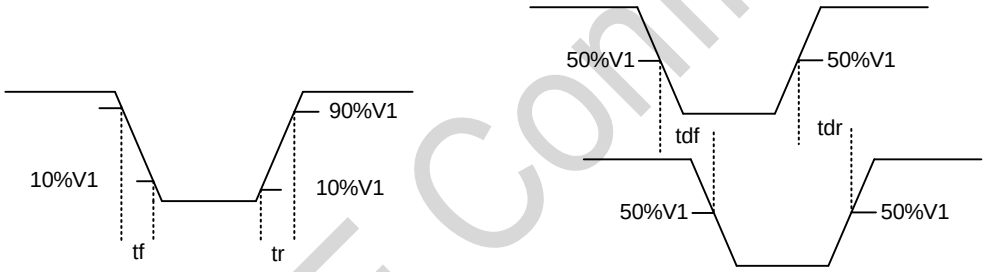


Figure 1-16-3. I/O AC Characteristic Definition

1.17 MCU_NRST Pin Characteristics

MCU_NRST pin input driver uses CMOS technology. MCU_NRST pin is connected to a pull-up resistor that cannot be disconnected.

Table 1-17-1. NRST Pin Characteristics

Symbol	Parameter	VDD	Min	Typ	Max	Unit	Symbol
$V_{IL(NRST)}$(1)	NRST low level input voltage	2.0V~3.6V	--	--	--	$0.3V_{DD}$	V
$V_{IH(NRST)}$(1)	NRST high level input voltage	2.0V~3.6V	--	$0.75V_{DD}$	--	--	
$V_{hys(NRST)}$	NRST schmitt trigger voltage hysteresis	2.0V~3.6V	--	115	220	315	mV
$V_{OL(NRST)}$(1)	NRST output low level voltage	3.3V	High driving Imin=8mA low driving Imin=4mA	--	--	0.45	V
		2.0V	High driving Imin=4mA low driving Imin=2mA	--	--	0.4	
$V_{OH(NRST)}$ (1)	NRST output high level voltage	3.3V	High driving Imin=8mA low driving Imin=4mA	2.4	--	--	
		2.0V	High driving Imin=4mA low driving Imin=2mA	VDD-0.45	--	--	
R_{PU}	Internal pull-up resistor(2)	2.0V~3.6V	--	30	60	70	kΩ
$V_{F(NRST)}$(1)	NRST input filter pulse	2V	--	--	--	100	ns
		3V~3.6V	--	--	--	100	
$V_{NF(NRST)}$(1)	NRST input unfiltered pulse	2V	--	650	--	--	ns
		3V~3.6V	--	300	--	--	

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. The pull-up resistor is designed for a resistor in series with a non-switchable PMOS. The resistance of this PMOS switch is rather small (it is about 10%).

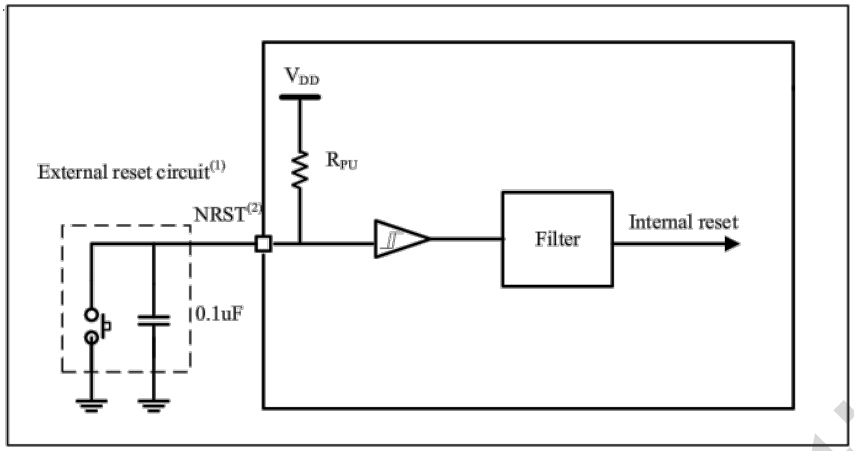


Figure 1-17-2. NRST Pin Protection Recommended Circuit Design

1. The reset network is to prevent parasitic reset.

2. Users must ensure that the potential of the NRST pin can be lower than the maximum VIL (NRST), otherwise MCU cannot be reset.

1.18 TIM Characteristic

Table 1-18-1. TIMx(1) Characteristic

Symbol	Parameter	Conditions	Min	Max	Unit
tres(TIM)	Timer resolution time	--	1	--	tTIMxCLK
		fTIMxCLK= 48MHz	20.8	--	ns
fEXT(2)	Timer external clock frequency from CH1 to CH4	--	0	fTIMxCLK/2	MHz
		fTIMxCLK= 48MHz	0	24	MHz
ResTIM	Timer resolution	--	--	16	Bits
tCOUNTER	Select the internal clock, 16-bit counter clock cycle	--	1	65536	tTIMxCLK
		fTIMxCLK= 48MHz	0.0208	1365	μs
tMAX_COUNT	Maximum count	--	--	2^16x2^16	tTIMxCLK
		fTIMxCLK= 48MHz	-	89.478	s

1. X can be 1,3,6.

2. TIM1 is CH1~CH4，TIM3 is CH1~CH2，while it is not applicable to TIM6.

1.19 IWDG Characteristic

Table 1-19. Max and Min Counter Reset Time of IWDG（LSI=32kHz）

Predivision	IWDG_PREDIV.PD[2:0]	Min(1) IWDG_RELV.REL[11:0]=0	Max(1) IWDG_RELV.REL[11:0]=0xFFF	Unit
/4	3'b000	0.125	512	ms
/8	3'b001	0.25	1024	
/16	3'b010	0.5	2048	
/32	3'b011	1	4096	
/64	3'b100	2	8192	
/128	3'b101	4	16384	
/256	3'b11x	8	32768	

1. Guaranteed by design and comprehensive evaluation, not tested in production.

1.20 I²C Interface Characteristic

The I2C interface complies with the standard I2C communication protocol while SDA and SCL are not "true" open-drain pins. When configured as open-drain output, the PMOS tube between the pin and VDD will be turned off, but still exists.

The I2C interface characteristic is shown as the following table. As for the specification of I/O reset function pins (SDA and SCL), please refer to chapter 1.16

Table 1-20-1. I²C Characteristics

Symbol	Parameter	Standard model		Fast mode		Fast + mode		Unit
		Min	Max	Min	Max	Min	Max	
f^{SCL}	I2C interface frequency	0	100	0	400	0	1000	KHz
$th_{(STA)}$	Start condition holding time (1)	4.0	-	0.6	-	0.26	-	μs
$t_{w(SCLL)}$	SCL Clock Low Time (1)	4.7	-	1.3	-	0.5	-	μs
$t_{w(SCLH)}$	SCL clock high time (1)	4.0	-	0.6	-	0.26	-	μs
$t_{su(STA)}$	Establishment time of repeated starting conditions (1)	4.7	-	0.6	-	0.26	-	μs
$t_{h(SDA)}$	SDA data retention time (1)	-	3.4	-	0.9	-	0.4	μs
$t_{su(SDA)}$	Establishment time of SDA (1)	250	-	100	-	50	-	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time (1)	-	1000	20+0. 1Cb	300	-	120	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time (1)	-	300	20+0. 1Cb	300	-	120	ns
$t_{su(STO)}$	Establishment time of stop condition(1)	4.0	-	0.6	-	0.26	-	μs
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus idle) (1)	4.7	-	1.3	-	0.5	-	μs
Cb	Capacity load per bus (1)	-	400	-	400	-	200	pf
$t_{v(SDA)}$	Data validity time(1)	3.45	-	0.9	-	0.45	-	μs

$t_{v(ACK)}$	Response validity time (1)	3.45	-	0.9	-	0.45	-	μs

1. Guaranteed by design and comprehensive evaluation, not tested in production.

2. To achieve the maximum frequency of standard mode I2C, F_{PCLK1} must be greater than 2 MHz.To achieve the maximum frequency of fast mode I2C, F_{PCLK1} must behigher than 4 MHz.

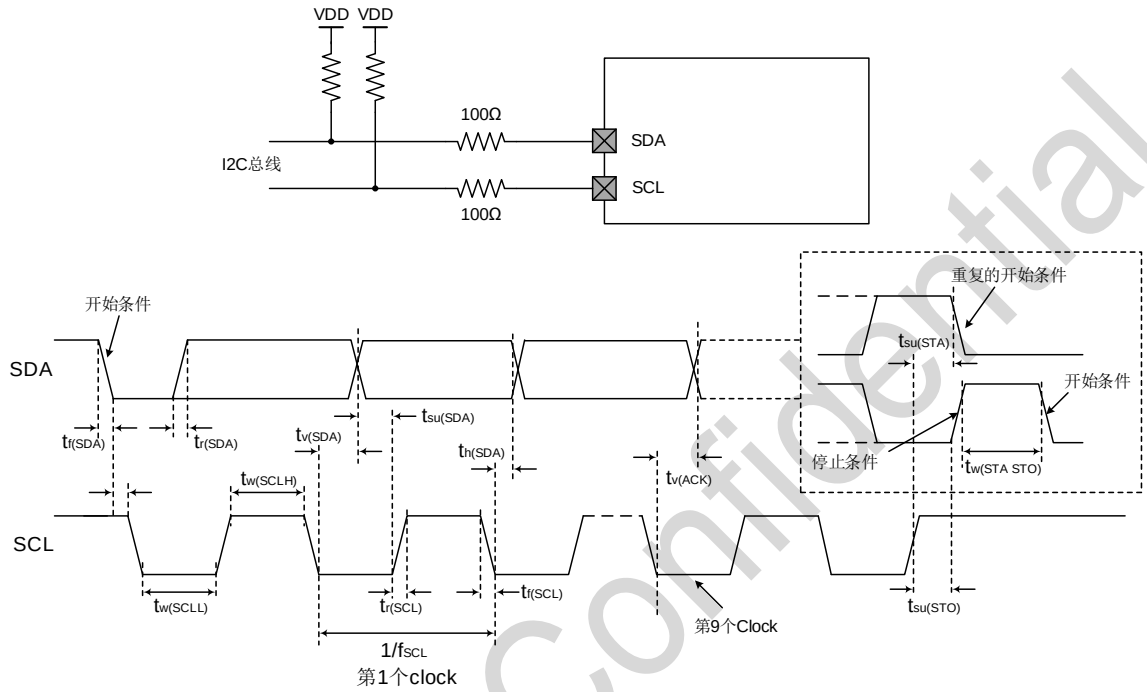


Figure 1-20-2. I²C Bus AC Waveform and Measurment Circuit (1)

1. The measuring point is set at CMOS level: 0.3 VDD and 0.7 VDD.

2. The pull-up resistor value depends on the I2C interface speed.

3. The resistance value depends on the actual electrical characteristics, it can be discontinuous serial resistance and connect to the signal line directly.

1.21 SPI Characteristic

For feature details of the input and output multiplexing pins（NSS、SCLK、MOSI、MISO of SPI）, see Section 1.16.

Table 1-21-1. SPI Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCLK} $1/t_{c(SCLK)}$	SPI clock frequency	Master mode	--	12	MHz
		Slave mode	--	12	
$t_{r(SCLK)}t_{f(SCLK)}$	SPI clock rise and fall time	Load capacitance：C = 30pF	--	15	ns
DuCy(SCLK)	SPI slave input clock duty cycle	SPI Slave mode	30	70	%
$t_{su(NSS)}$ (1)	NSS establishment time	Slave mode	$4t_{PCLK}$	--	ns
$t_{h(NSS)}$(1)	NSS retention time	Slave mode	$2t_{PCLK}$	--	ns

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{w(SCLKH)}$(1) $t_{w(SCLKL)}$(1)	SCLK high and low time	Master mode	t_{PCLK}	t_{PCLK} + 2	ns
$t_{su(MI)}$(1)	Data input setup time	Master mode	5	--	ns
$t_{su(SI)}$(1)		Slave mode	5	--	
$t_{h(MI)}$(1)	Data input retention time	Master mode	5	--	ns
$t_{h(SI)}$(1)		Slave mode	4	--	
$t_{a(SO)}$(1)(2)	Data output access time	Slave mode	0	$3t_{PCLK}$	ns
$t_{dis(SO)}$(1)(3)	Data output disable time	Slave mode	2	10	ns
$t_{v(SO)}$(1)	Data output validity time	Slave mode (after the enabled edge)	-	5	ns
$t_{v(MO)}$(1)		Master mode (after theenabled edge)	-	5	
$t_{h(SO)}$(1)	Data output retention time	Slave mode (after the enabled edge)	15	-	ns
$t_{h(MO)}$(1)		Master mode (after theenabled edge)	2	-	

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. The minimum value means the minimum time to drive the output, and the maximum value means the maximum time to get the data correctly.
3. The minimum value means the minimum time to turn off the output, and the maximum value means the maximum time to put the data line in the high resistance state.

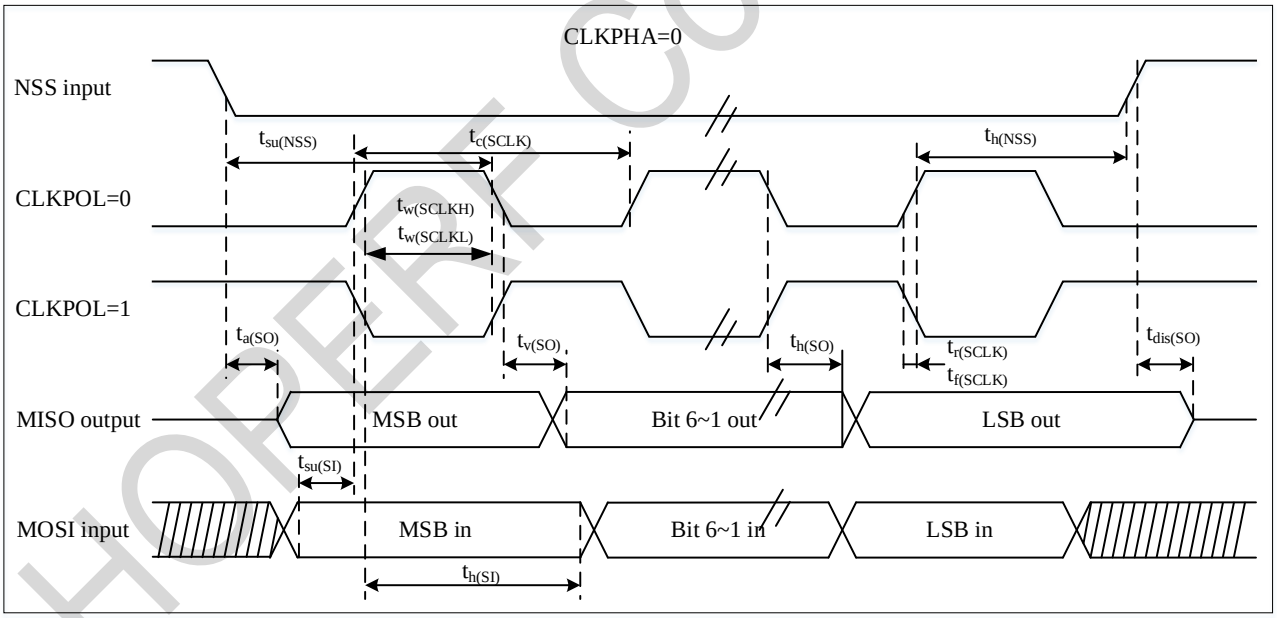


Figure 1-21-2.SPI Sequence Diagram – Slave Mode and CPHA=0

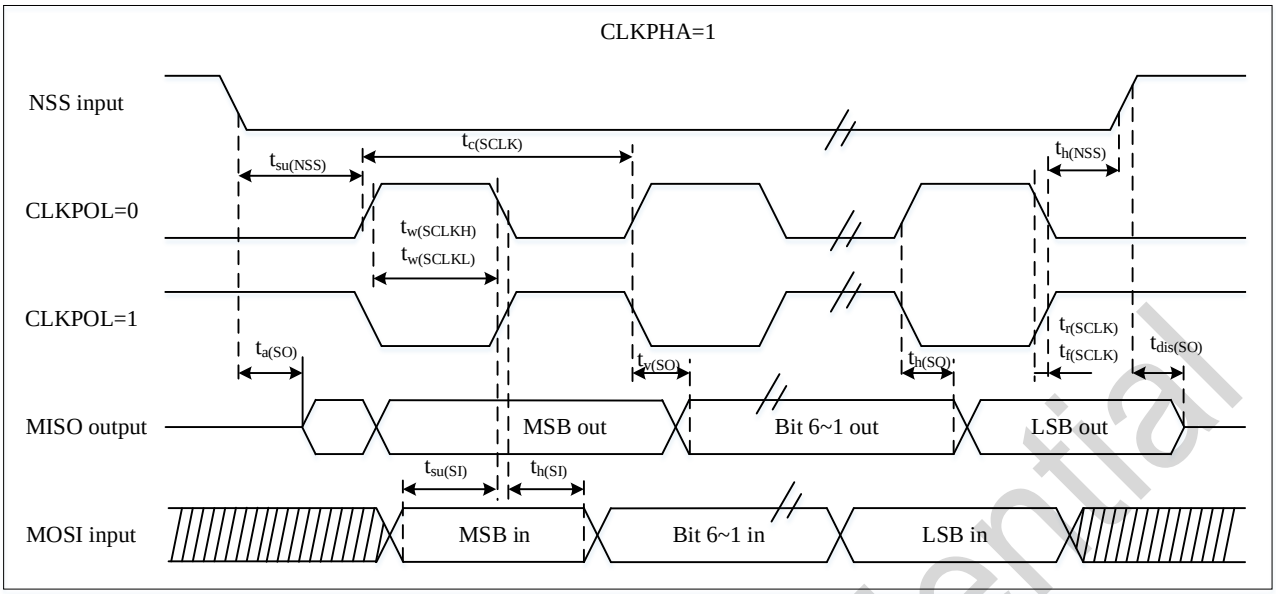


Figure 1-21-3.SPI Sequence Diagram - Slave Model and CPHA=1(1)

1. The measurement points are set at CMOS level: 0.3 VDD and 0.7 VDD.

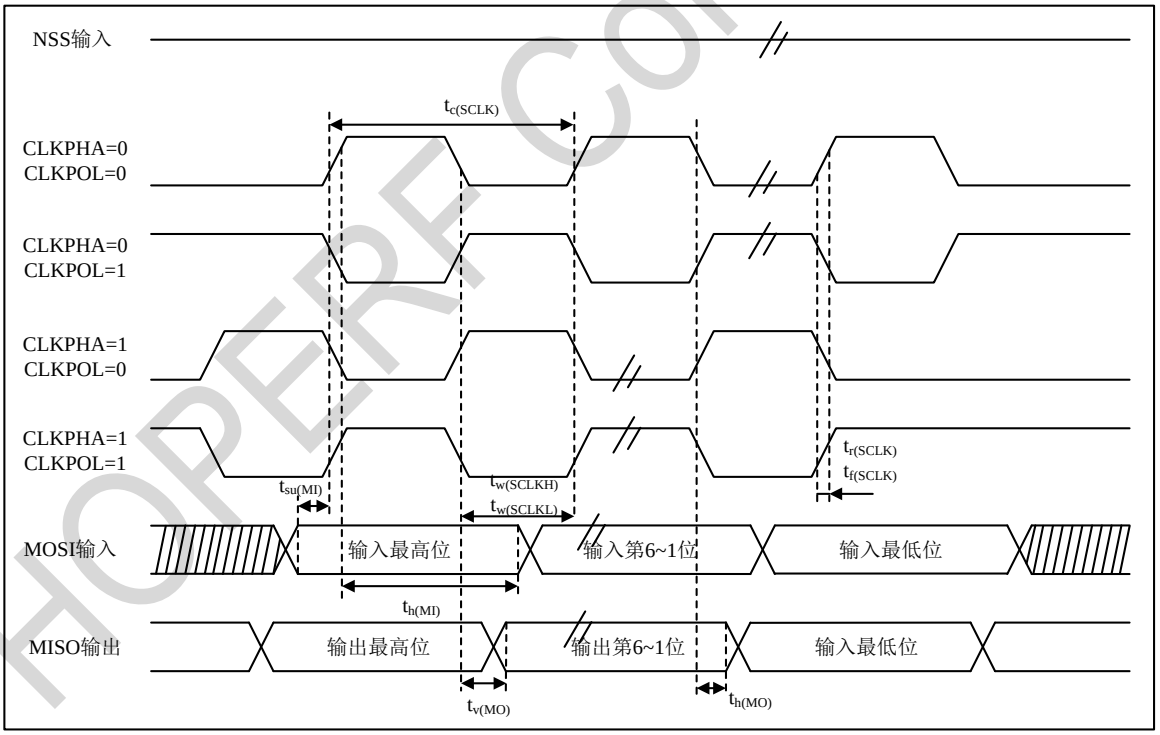


Figure 1-21-4. SPI Sequnece Diagram – Master Mode(1)

1. The measurement points are set at CMOS level: 0.3 VDD and 0.7 VDD.

1.22 ADC Characteristic

Table 1-22-1. ADC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Supply voltage	-	2.4	3.3	5.5	V
V_{REF+}	Positive reference voltage	-	-	-	-	V
f_{ADC}	ADC clock frequency	-	-	-	24	MHz
f_s(1)	Sampling rate	-	0.03	-	1	Msps
V_{AIN}	Conversion voltage range (2)	-	0	-	V_{REF+}	V
R_{AIN}(1)	External input impedance	-	参见公式1			Ω
R_{ADC}(1)	ADC input resistance	V_{DDA} = 3.0v	-	1500	-	Ω
C_{ADC}(1)	Internal sample and holding capacitor	-	-	26	-	pF
SNDR	Singal noise distortion ration	V_{DDA} = 3.3v	-	58.5	-	dB
t_S(1)	Sampling time	-	6	-	-	$1/f_{ADC}$
t_{STAB}(1)	Power-on time	-	32	-	-	$1/f_{ADC}$
t_{CONV}(1)	Conversion time	-	12			$1/f_{ADC}$
I_{ADC}	ADC current consumption	-	-	1.67	-	mA

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. VREF+ is internally connected to VDDA。

Formula 1：maximum RAIN formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The above formula is used to determine the maximum impedence so that the error can be less than 1/4 LSB, where N=12 (representing 12-bit resolution).

Table 1-22-2. ADC Sampling Time

Resolution	Rin（kΩ）	Min Sampling time（ns）
12-bit	1	500
	1.2	583
	2	833
	3.6	1250
	8.26	2333
	10	3000
	18	5000
	26.9	7583
	35.9	10000
	61.9	15833

1. Guaranteed by design, not tested in production.

Table 1-22-3. ADC Accuracy (1)(2)

Symbol	Parameter	Conditions	Typ	Max	Unit
EG	Gain error	V_{REF+} = 3.3 V，T_A = 25 °C，sample rate=1 Vin = 0.05 V_{DDA}~ 0.95 V_{DDA}	±2	±5	LSB
EO	Offset error		±0.5	±2.0	
ED	Differential linearity error		±0.6	1.5	
EL	Integral linearity error		±1.5	2.5	
ENOB	Effective number of bits		9.4	-	Bits

1. DC numerical accuracy of the ADC is measured after internal calibration.
2. Relationship between the reverse injection current and ADC accuracy: it is needed to avoid reverse current injected on any standard analog input pin, as this will significantly reduce conversion accuracy of the other ongoing analog input pin. It is recommended to add a Schottky diode (between the pin and ground) on the standard analog pin that may produce reverse injection current.
3. Guaranteed by design and comprehensive evaluation, not tested in production.

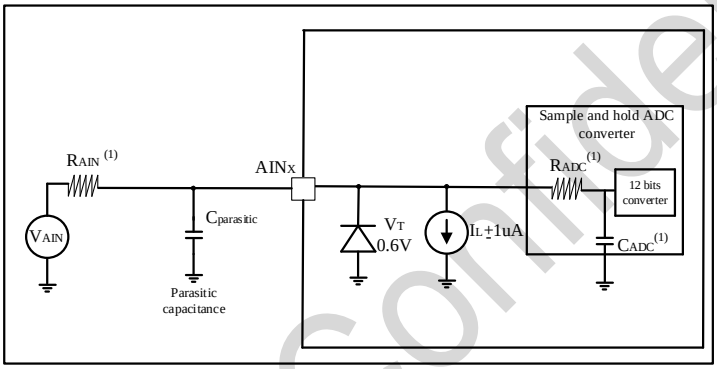


Figure 1-22-4. ADC Typical Connection Diagram

1. For the values of R_{AIN}、R_{ADC} and C_{ADC}, see Table 1-22-1.
2. Cparasitic represents parasitic capacitance of the PCB (related to solder and PCB layout quality) and pad (approximately 7pF). The larger the Cparasitic values the lower the accuracy conversion, therefor the way to increasing accuracy is by reducing the value of f_{ADC}.

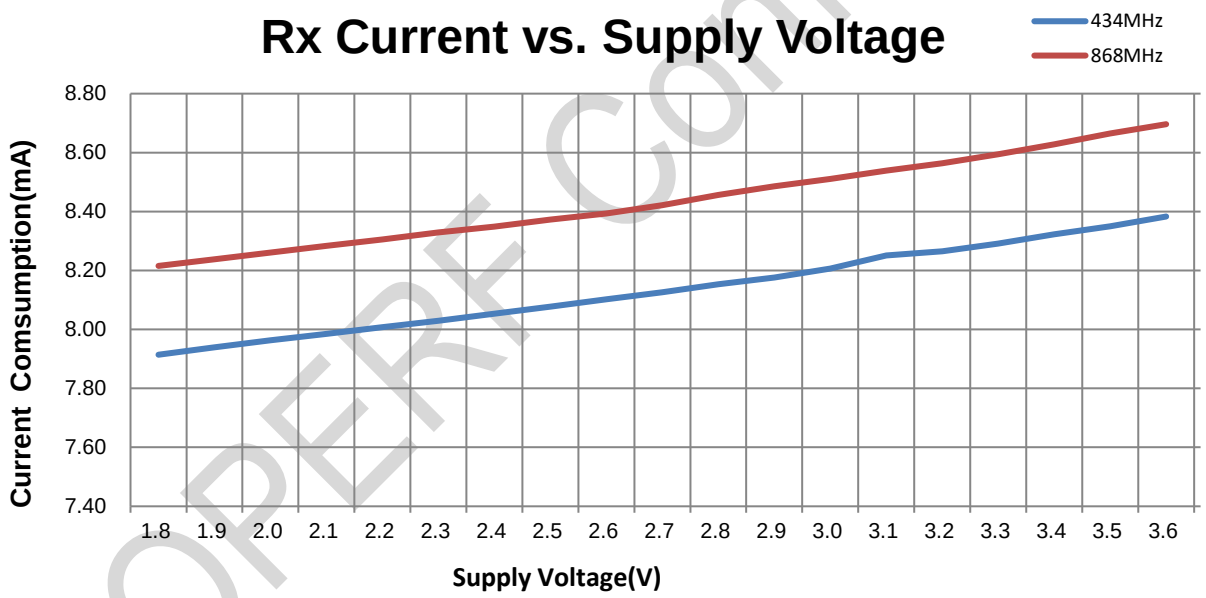
1.23 Comparator (COMP) Electrical Parameter

Table 1-23-1. COMP Characteristic

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Analog supply voltage	normal mode	2.4	-	5.5	V
		low speed mode	2.4	-	5.5	
V_{IN}	Analog supply voltage	V_{IN}	0	-	VDD	
		V_{IN} - 100mV/200mV/300mV	500	-	VDD-200	mV
t_{START}(1)	Comparator startup time	normal mode	-	-	5	μs
		low speed mode	-	-	15	
t_d	Propagation delay for 200mV step with 100m overdrive	Falling edge	-	304	-	ns
		Rising edge	-	268	-	
V_{OFFSET}	Comparator input offset error	VIN	-10	-	10	mV
		VIN - 100mV	-15	-	15	

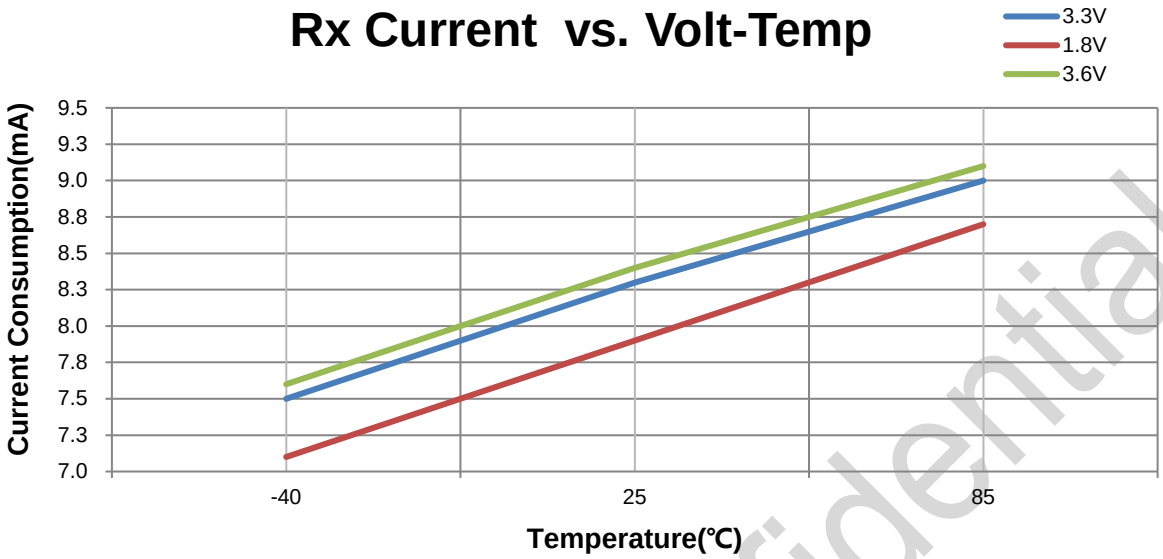
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		VIN - 200mV		-20	-	20	
		VIN - 300mV		-30	-	30	
V_{hys}	Comparison of hysteresis voltage	No hysteresis		-	0	-	mV
		Low hysteresis		-	10	-	
		Medium hysteresis		-	20	-	
		High hysteresis static		-	30	-	
I_{DD}	Comparator current consumption	normal mode	With 50kHz ±100 mV overdrive square signal static	-	-	50	μA
				-	-	50	
		Low speed mode	With 50 kHz ±100 mV overdrive square signal	-	-	500	
				-	-	500	
1. Guaranteed by design and comprehensive evaluation, not tested in production.							

1.24 Rx Current VS. Supply Voltage

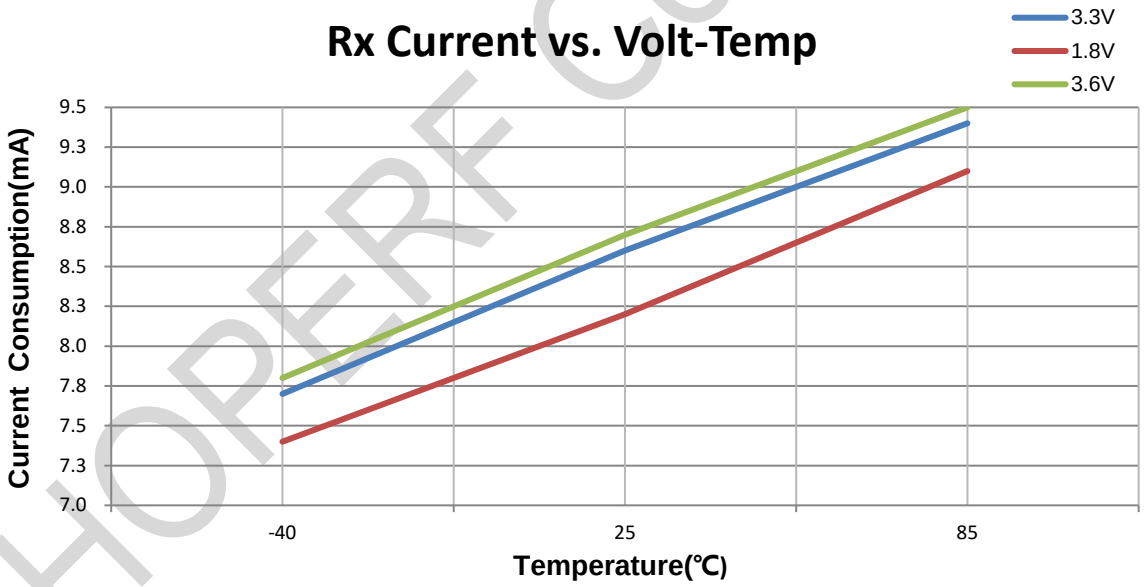


Test condition：Freq=434MHz / 868MHz，Fdev=10KHz，BR=10Kbps

1.25 Rx Current / Voltage vs. Temperature

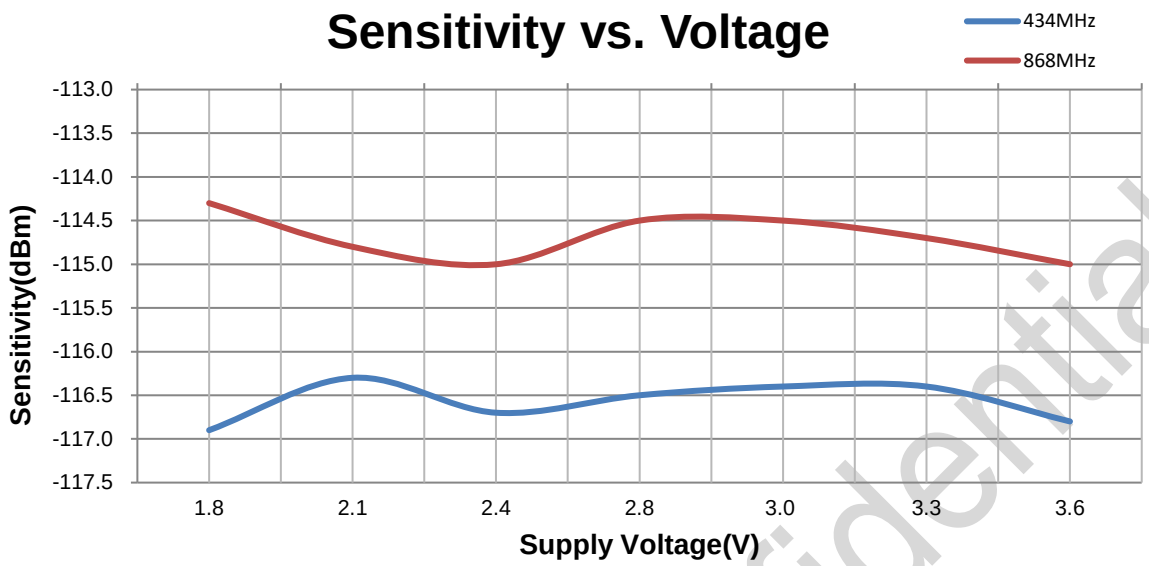


测试条件：Freq = 434MHz，Fdev = 10KHz，BR = 10Kbps



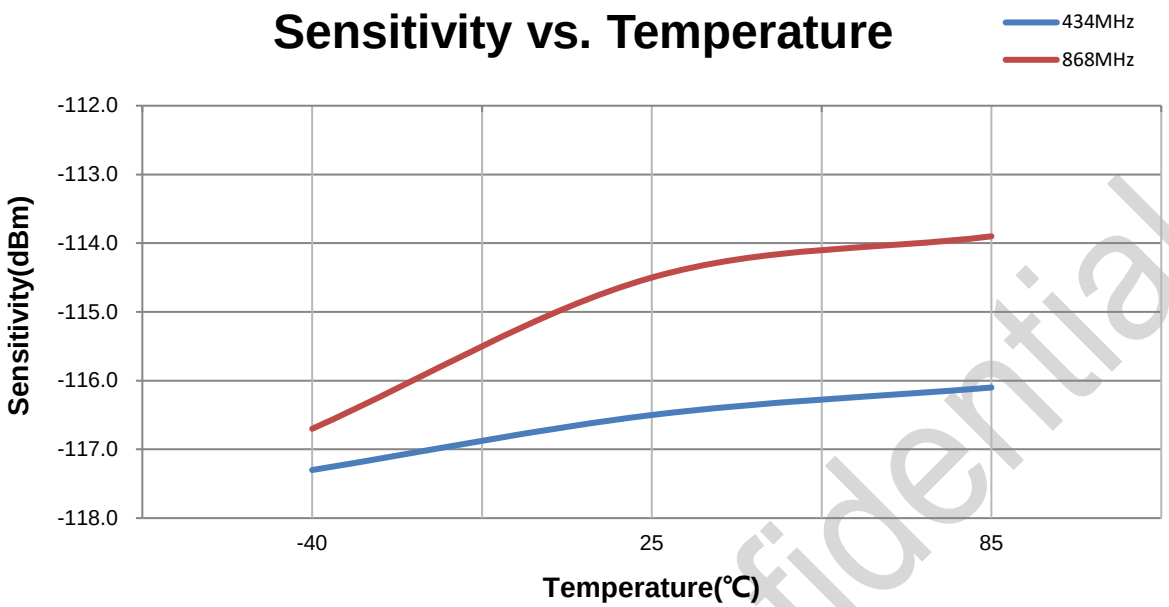
Test Condition：Freq = 868MHz，Fdev = 10KHz，BR = 10Kbps

1.26 Sensitivity vs. Supply Voltage



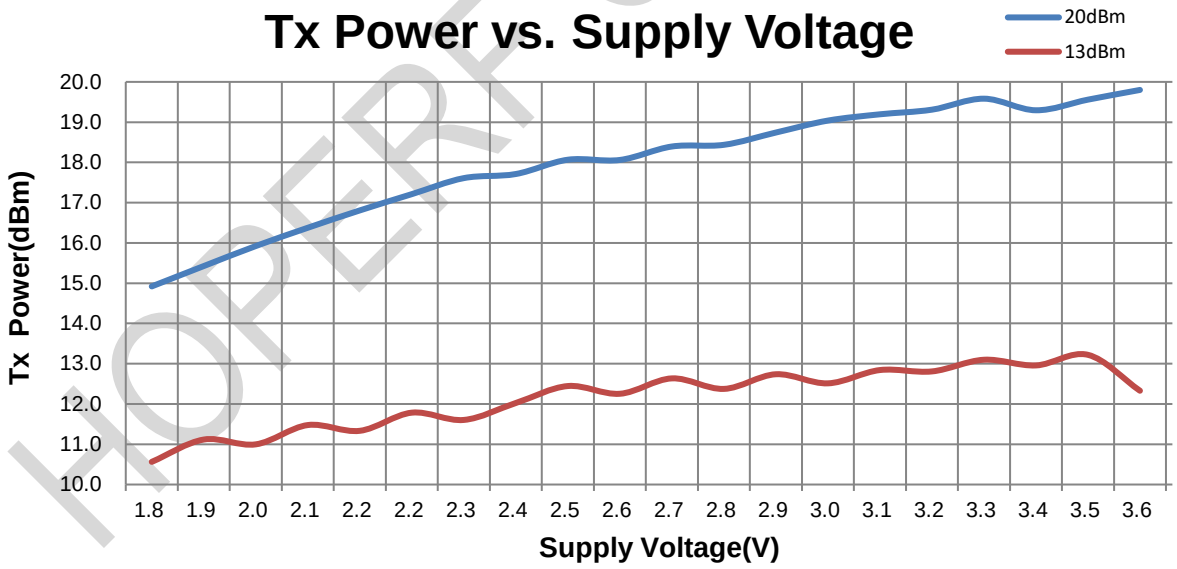
Test Condition：FSK modulation, DEV = 10KHz, BR = 10Kbps

1.27 Sensitivity vs. Temperature

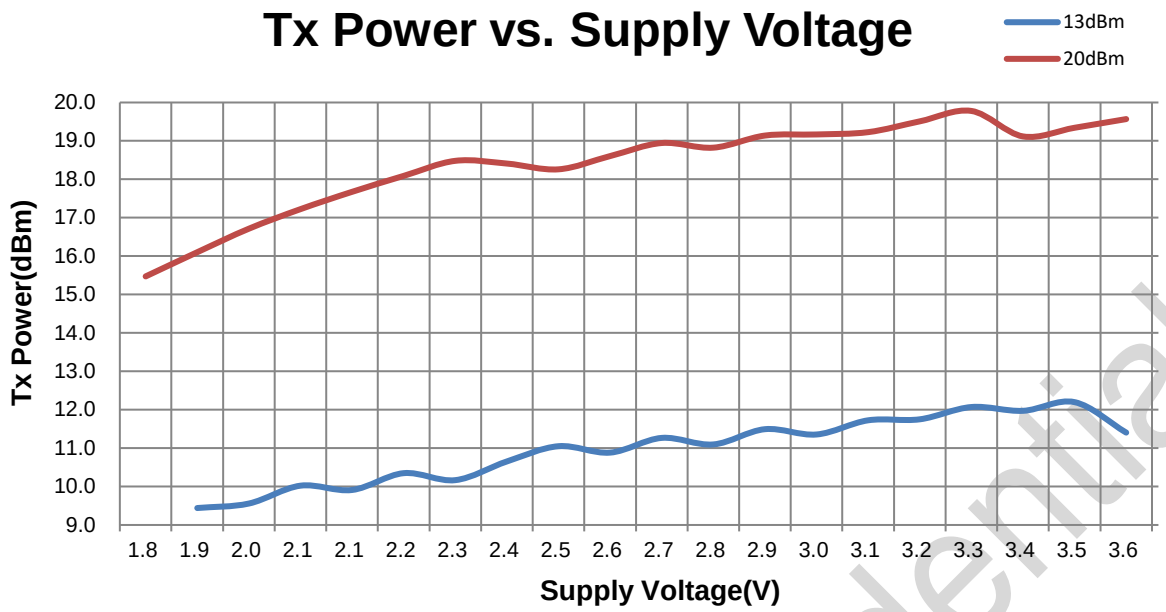


Test Condition：FSK modulation, DEV = 10KHz, BR = 10Kbps

1.28 Tx Power vs. Supply Voltage

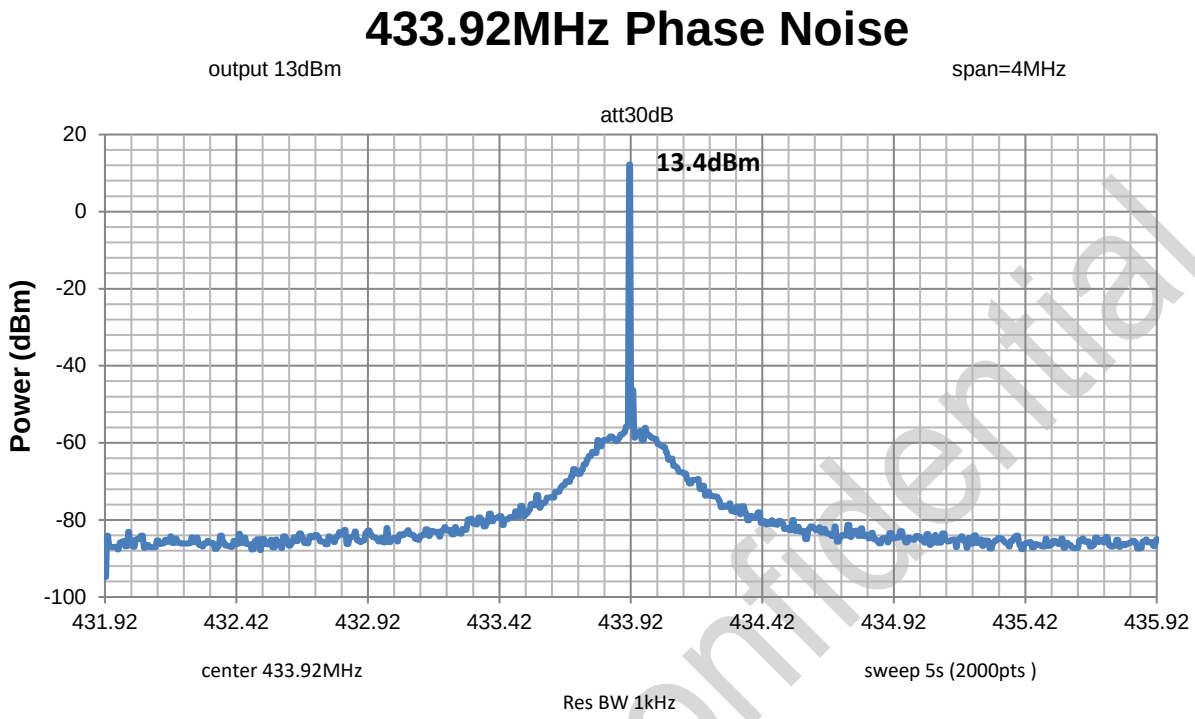


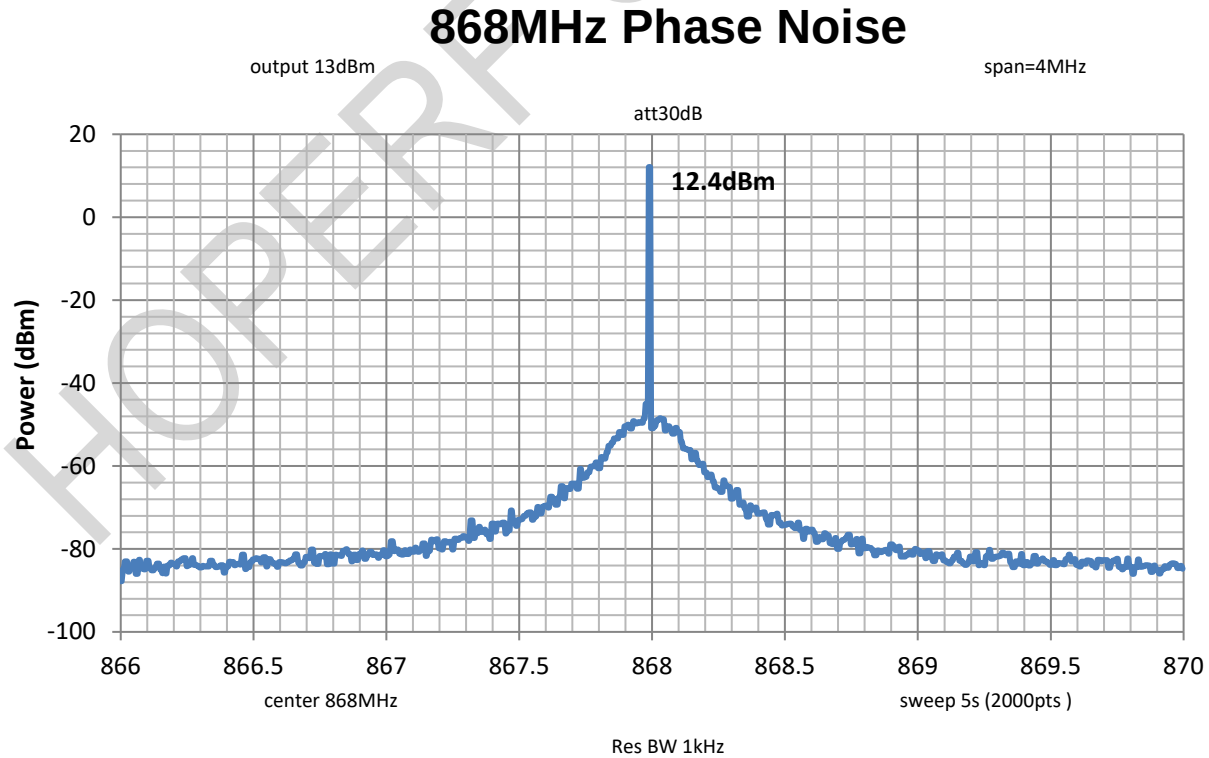
Test Condition：Freq = 434MHz, 20dBm / 13dBm matching network



Test Condition：Freq = 868MHz, 20dBm / 13dBm matching network

1.29 Tx Phase Noise





2 Pin Description

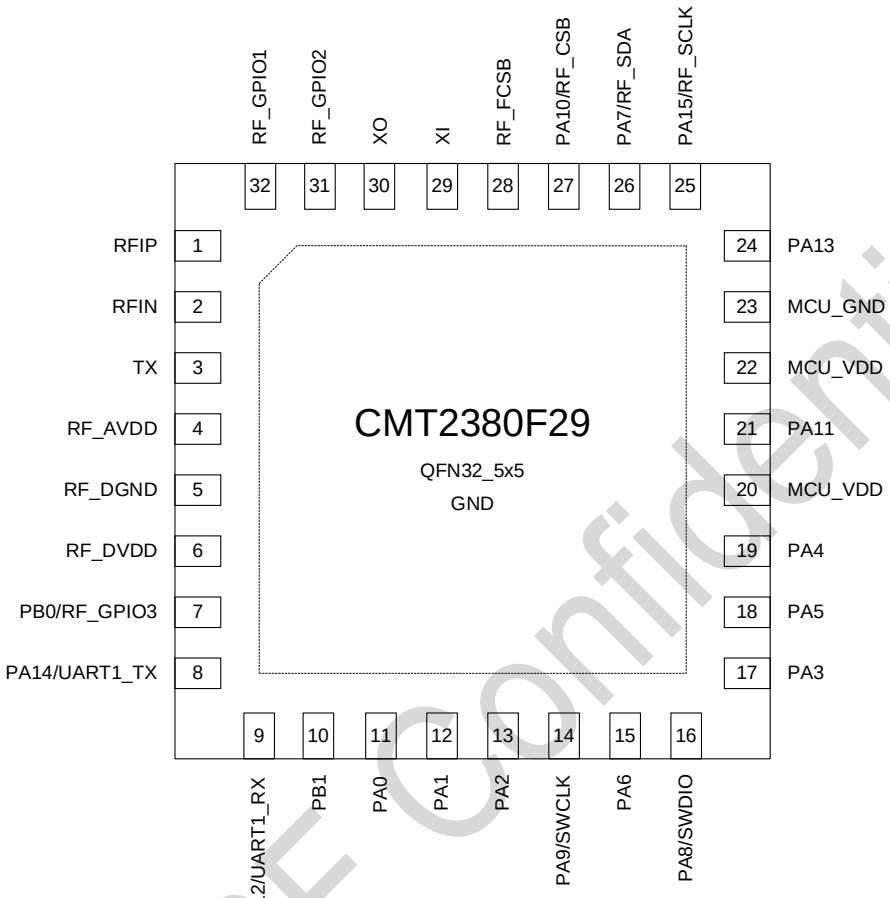


Figure 2-1. CMT2380F29-EQR Pin Diagram

Table 2-1. CMT2380F29 Pin Description

Pin No.	Pin Name	I/O	Description
1	RFIP	Analog	RF signal input port
2	RFIN	Analog	RF signal input port
3	TX	Analog	Data transmission
4	RF_AVDD	Analog	RF circuit VDD, required to connect to supply voltage of 2.0-3.6 V
5	RF_DGND	Analog	RF module digital GND
6	RF_DVDD	Analog	RF module digital VDD, required to connected to supply voltage of 2.0-3.6 V
7	PB0/RF_GPIO3	I/O	UART1_TX SPI_MISO TIM1_CH1 BEEPN EVENT_OUT AIN7

Pin No.	Pin Name	I/O	Description
			COMP_INP RF_GPIO3（internal connect）
8	PA14	I/O	TIM1_CH2 TIM3_CH1 TIM3_CH2 TIM1_CH4 TIM1_ETR UART1_TX SPI_SCK BEEP AIN6
9	PA12	I/O	TIM1_CH2 TIM1_CH2N TIM3_CH1 TIM3_CH2 TIM1_CH4 UART1_RX AIN4
10	PB1	I/O	UART1_RX SPI_MOSI TIM1_CH4 TIM3_ETR EVENT_OUT AIN8 COMP_INM
11	PA0	I/O	Can be configured as an NRST pin or a normal IO pin
12	PA1	I/O	UART2_RX I2C_SDA TIM1_CH3 TIM3_CH1 TIM1_BKIN WKUP0 AIN0
13	PA2	I/O	UART1_TX UART2_TX I2C_SCL TIM1_CH3N TIM3_CH2 WKUP1 AIN1
14	PA9	I/O	SWCLK UART2_TX I2C_SCL TIM1_BKIN TIM3_ETR
15	PA6	I/O	SPI_MOSI TIM1_CH1 TIM1_CH2N TIM3_CH1 TIM3_CH2 TIM1_CH4 TIM3_ETR

Pin No.	Pin Name	I/O	Description
16	PA8	I/O	SWDIO UART2_TX I2C_SDA SPI_NSS TIM1_CH4 COMP_OUT
17	PA3	I/O	UART1_RX SPI_NSS TIM1_CH3N TIM3_CH1 TIM3_CH2 TIM1_CH4
18	PA5	I/O	I2C_SDA TIM1_BKIN TIM1_CH1N AIN2 COMP_INP
19	PA4	I/O	I2C_SCL TIM1_CH3N EVENT_OUT COMP_INM
20	MCU_VDD	Analog	Power supply
21	PA11	I/O	TIM1_CH1 TIM1_CH1N TIM1_CH3 TIM3_CH1 TIM3_CH2 TIM1_CH4
22	MCU_VDD	Analog	Power supply
23	MCU_GND	Analog	MCU GND
24	PA13	I/O	MCO TIM1_CH1N TIM1_CH2N TIM1_CH4 TIM3_CH1 TIM3_CH2 AIN5
25	PA15/RF_SCLK	I/O	SPI_SCK TIM1_CH2 TIM1_ETR TIM3_CH1 TIM3_CH2 TIM1_CH4 RF_SCLK（internal connect ）
26	PA7/RF_SDA	I/O	SPI_MISO TIM1_CH2 TIM1_CH3 TIM3_CH1 TIM3_CH2 TIM1_CH4 UART2_RX RF_SDA（internal connect）

Pin No.	Pin Name	I/O	Description
27	PA10/RF_CSB	I/O	TIM1_CH3 TIM1_CH3N TIM3_CH1 TIM3_CH2 TIM1_CH4 AIN3 RF_CSB（internal connect）
28	RF_FCSB	I	Access FIFO segment of RF SPI
29	XI	I	26 MHz crystal circuit input
30	XO	O	26 Mhz crystal circuit output
31	RF_GPIO2	I/O	RF module GPIO2, can be configured as：INT1，INT2，DOUT/DIN，DCLK (TX/RX)，RF_SWT
32	RF_GPIO1	I/O	RF module GPIO1, can be configured as：DOUT/DIN，INT1，INT2，DCLK (TX/RX)，RF_SWT

3 Chip Frame

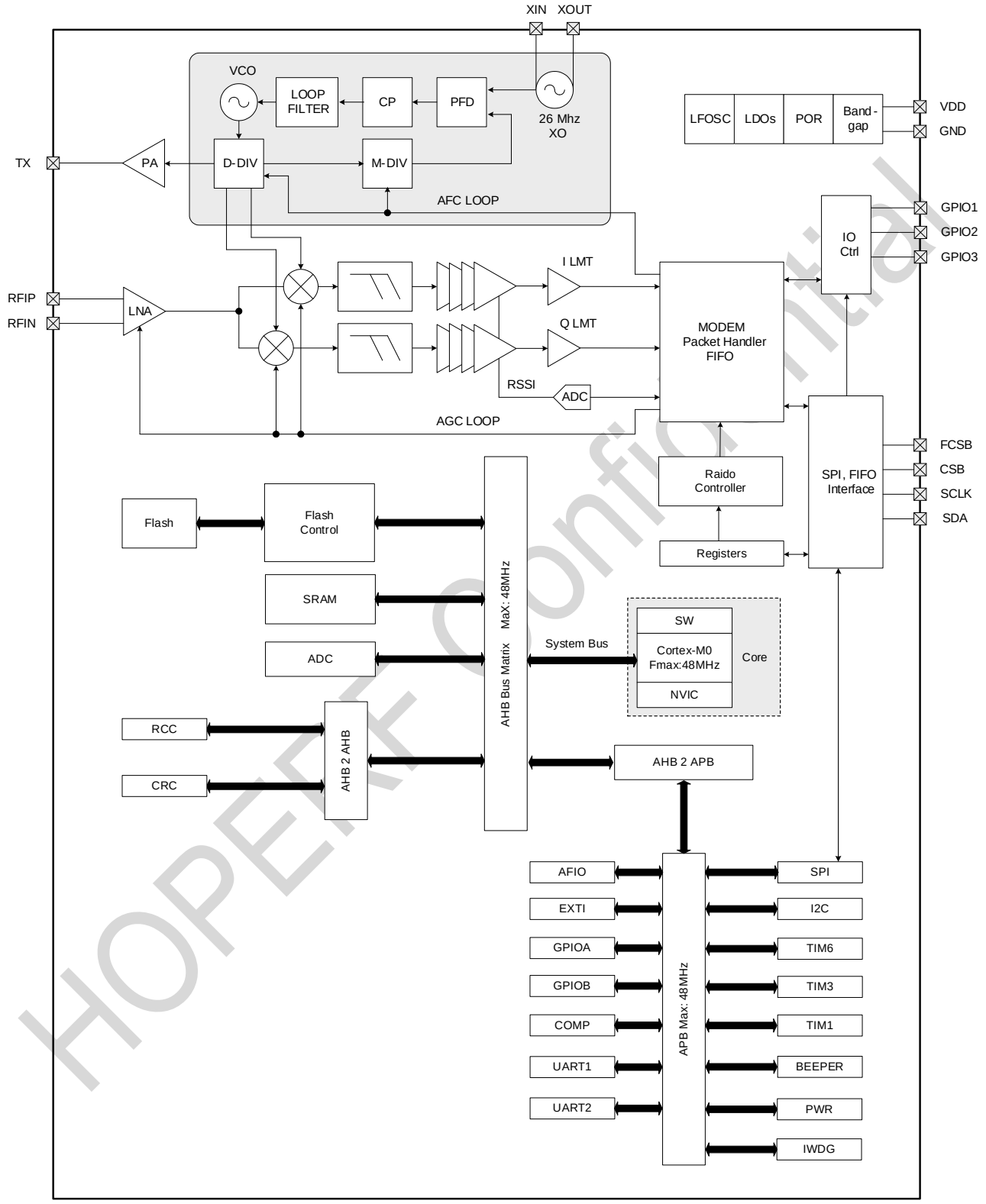


Figure 3-1. Functional Block Diagram

CMT2380F29 is an integrated Sub-G high-performance wireless transceiver single chip. The internal system block diagram of CMT2380F29 is shown above at figure 3-1.

- Low power high performance Sub-G transceiver

Sub-G wireless transceiver supports 127 to 1020 MHz, OOK, (G)FSK,(G)MSK and other modulation modes, low power consumption, high performance, suitable for all kinds of wireless communication applications. The product belongs to CMOSTEK Next GenRFTM series, which includes transmitters, receivers and transceivers and other complete product series.

- ARM Cortex-M0 high performance 32e bit micro-processor

The CMT2380F29 controller uses a 32-bit ARM Cortex®-M0 kernel, with a maximum operating frequency of 48MHz, up to 29.5KB encrypted Flash memory integrated, and a maximum of 3KB SRAM. Built-in a high-speed AHB bus, two low-speed peripherals APB and bus matrix, support up to 18 general I/O, provide several high-performance analog interfaces, including a 12-bit 1Msps ADC, up to 12 external input channels, 1 independent operational amplifier, 1 high-speed comparator, and provides a variety of digital communication interfaces, including two U(S)ART, one I^2C and one SPI.

The CMT2380F29 resources are shown as followed.

Table 3-1. CMT2380F29 External Resources

Project Name		CMT2380F29 External Resources	Notes
Flash capacitance（KB）		29.5	
SRAM capacitance（KB）		3	
CPU kernal and frequency		ARM Cortex-M0 @ 48MHz	
Operating environment		2.0～3.6V / -40～+85℃	
Timer	General	3	
	High level	16 interrupt sources, 4 level priority	
	Basic	Enhance serial port	
	LPTIM	Support	
Communication interface	SPI	Support	
	I2C	Support	
	USART	x2	
GPIO		18	4 of them are connected to the RF of SPI and GPIO3
12bit ADC		9-ch	1Msps
COMP		1 / 1	

Beeper	1	
Algorithmic support	CRC16	
Security protect	Read/write protect（RDP / WRP）,Storage encryption	

4 Sub-G Transceiver

4.1 Transmitter

The transmitter is based on direct frequency synthesis technology. The carrier is generated by a low noise fractional-N frequency synthesizer. The modulated data is transmitted by an efficient single-ended power amplifier (PA). The output power can be read and written via registers, step by step from -20 dBm to +20 dBm with 1 dB.

When the PA is switched fast, the varying input impedance will disturb the output frequency of the VCO instantaneously. The effect is called VCO pulling. It will generate the spurious and spurson the spectrum around the desired carrier. The PA spurs can be reduced to a minimum instantaneously by the PA output power ramping. CMT2380F64 has a built-in PA ramping mechanism. When the PA Ramp is turned on, the PA output power can ramp the desired amplitude in a pre-configuredrate, so as to reduce the spurs. In FSK mode, the signal can be filtered by a Gaussian Filter before transmitted, e.g. GFSK, which can reduce the spectral width and interference with neighboring channels.

According to different application requirements, users can design a PA matching network to optimize the transmitting efficiency. The typical application schematic and the required BOM is shown in Chapter 3 "Typical application schematic".

The transmitter can operate in direct mode and packet mode. In the direct mode, the data to be transmitted can be sent to the chip by the DIN pin and transmitted directly. In the packet mode, the data can be pre-loaded into the TX FIFO in STBY state, and transmitted together with other package elements.

4.2 Receiver

CMT2380F29 has a built-in ultra-low power, high performance low-IF OOK, FSK receiver. The RF signal induced by the antenna is amplified by a low noise amplifier, and is converted to an intermediate frequency by an orthogonal mixer. The signal is filtered by the image rejection filter, and is amplified by the limiting amplifier and then sent to the digital domain for digital demodulation. During power on reset (POR) each analog block is calibrated to the internal reference voltage. This allows the chip to remain its best performance at different temperatures and voltages. Baseband filtering and demodulation is done by the digital demodulator. The AGC loop adjust the system gain by the broad band power detector and attenuation network nearby LNA, so as to obtain the best system linearity,selectivity, sensitivity and other performance.

Leveraging CMOSTEK's low power design technology, the receiver consumes only a very low power when it is turned on.The periodic operation mode and wake up function can further reduce the average power consumption of the system in the application with strict requirements of power consumption.

Similar to the transmitter, the CMT2380F29 receiver can operate in direct mode and packet mode. In the direct mode,the demodulator output data can be directly output through the DOUT pin of the chip.DOUT can be assigned to GPIO1/2/3. In the packet mode, the demodulator data output is sent to the data packet handler, get decoded and then fills into the FIFO. MCU can read the FIFO by the SPI interface.

4.3 Power-on Reset (POR)

The Power-On Reset circuit detect the change of the VDD power supply, and generate the reset signal for the entire CMT2380F29 system. After the POR, the MCU must go through the initialization process and re-configure CMT2380F29. There are two circumstances which will lead to the generation of POR.

The first case is a very short and sudden decrease of VDD. The POR triggering condition is, VDD dramatically decreases by 0.9V +/- 20% (e.g.0.72V–1.08V) within 2us. To be noticed, it detects a decreasing amplitude of the VDD, not the absolute value of VDD as shown in the below figure.

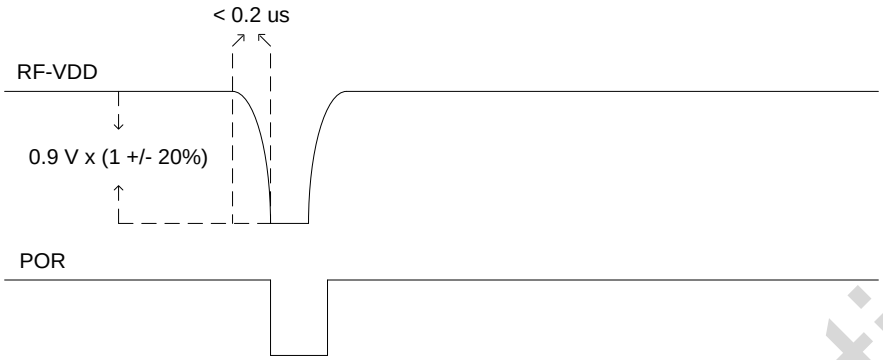


Figure 4-1. POR Reset Causing from Sudden Decreasing

The second case is a slow decrease of the VDD. The POR triggering conditionis, RF-VDD decreases to 1.45 V+/-20% (e.g.1.16 V–1.74 V) within no less than 2us. To be noticed, it detects absolute value of RF-VDD rather than decreasing amplitude. This situation is shown as below:

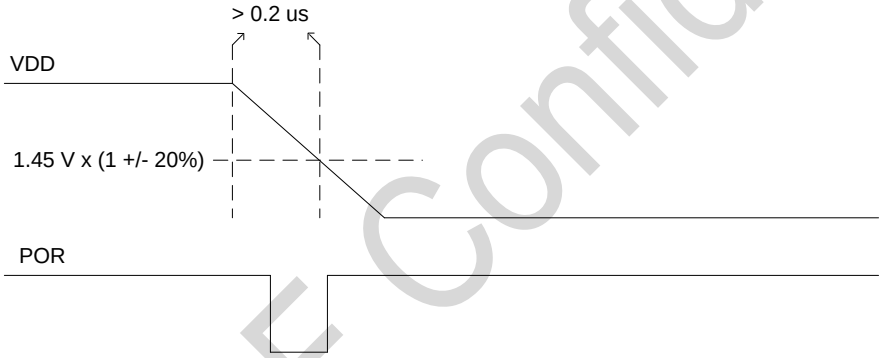


Figure 4-2. POR Reset Causing from Slow Decreasing

4.4 Crystal Oscillator

The crystal oscillator provides a reference clock for the phase locked loop as well as a system clock for the digital circuits. The value of load capacitance depends on the crystal specified CL parameters. The total load capacitance between XI and XO should be equal to CL to make the crystal accurately oscillate at 26 MHz.

$$\mathbf{C_L = \frac{1}{1/C15 + 1/C16} + C_{par} + 2.5pF}$$

C15 and C16 are the load capacitances at both ends of the crystal. Cpar is the parasitic capacitance on the PCB. Each crystal pin has 5pF internal parasitic capacitance, together is equivalent to 2.5pF. The equivalent series resistance of the crystal must be within the specifications so that the crystal can have a reliable vibration. Also, an external signal source can be connected to the XI pin to replace the conventional crystal. The recommended peak value of this clock signal is from 300mV to 700mV. The clock is coupled to XI pin via a blocking capacitor.

4.5 Low Power Frequency Oscillator（LPOSC）

The CMT2380F29 RF system integrates a sleep timer driven by a 32 kHz low power oscillator (LPOSC). When this function is enabled, the timer periodically wakes the chip from sleep. When the chip is operating in periodic operation mode, the sleep time can be configured from 0.03125 ms to 41,922,560 ms. Since the frequency of the low power oscillator will drift with temperature and voltage changes, it will be automatically calibrated during the power-up phase and will be periodically calibrated. Calibrations will keep the frequency tolerance of the oscillator within 1%.

4.6 Internal Low Power Detection

The chip sets up low voltage detection. When the chip is tuned to a certain frequency, test will be occured accordingly. Frequency tuning occurs when the chip jumps from the SLEEP/STBY state to the RFS/TFS/TX/RX state. The result can be read by the LBD_VALUE register.

4.7 Received Signal Strength Indicator（RSSI）

RSSI is used to evaluate the signal strength inside the channel. The cascaded I/Q logarithmic amplifier amplifies the signal before it is sent to the demodulator. The logarithmic amplifier of I channels and Q channel contains the received signal indicator, in which the DC voltage generated is proportional to the input signal strength. The output of RSSI is the sum of the values of the two channels' signals. The output has 80 dB dynamic range above the sensitivity. After the RSSI output is sampled by the ADC and filtered by a SAR filter and an average filter. The order of the average filter can be set by RSSI_AVG_MODE<2:0>. The code value is translated into dBm value after filtering. User can read the register RSSI_CODE<7:0> to obtain the RSSI code value, or RSSI_DBM<7:0> to obtain the dBm value. Users can determine whetherthe RSSI is output to the MCU in real time, or latched RSSI value while receiving packets in different states by setting the register RSSI_DET_SEL<1:0>.
CMT2380F29 allows user to setup threshold through RSSI_TRIG_TH<7:0> to compare with the real-time RSSI value. If the RSSI is larger than the threshold it outputs logic 1, otherwise it outputs logic 0. The output can be used as a source of the RSSI VLD interrupt of the receive time extending condition in the super-low power (SLP) mode.

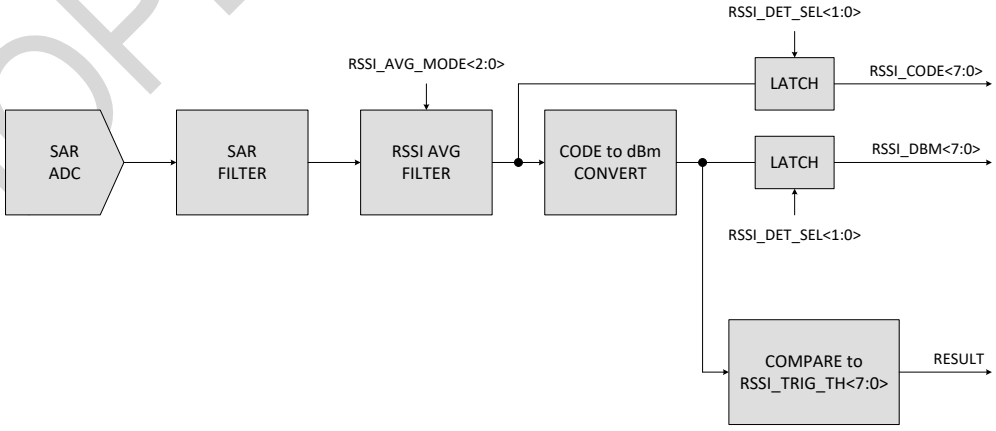


Figure 4-3. RSSI Detection and Comparison Circuit

CMT2380F29 has done a certain degree of calibration before delivery. In order to obtain more accurate RSSI measurement results, user needs to recalibrate the RSSI circuit during applications. For further information, please refer to the AN144-CMT2300A RSSI Usage Guideline.

4.8 Phase Jump Detector（PJD）

PJD is Phase Jump Detector. When the chip is in FSK demodulation, it can automatically observe the phase jump characteristics of the received signal to determine whether it is a wanted signal or an unwanted noise.

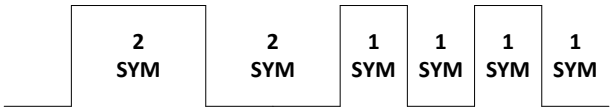


Figure 4-4. Received Signal Jump Diagram

The PJD mechanism defines that the input signal switching from 0 to 1 or from 1 to 0 is a phase jump. Users can configure the PJD_WIN_SEL<1:0> to determine the number of detected jumps for the PJD to identify a wanted signal. As shown in the figure above, 8 symbols are received. But the phase jump only appeared 6 times. Therefore, the number of jumps is not equal to the number of symbols. Only when a preamble is received and they are equal. In general, the more jumps of the signal, the more reliable the result is; the less jumps of the signal, the faster the result is obtained. If the RX timeis set to are latively short period, it is necessary to reduce the number of jumps to meet the timing requirements. Normally, 4 jumps allow pretty reliable result, e.g.the chip will not mistakenly treat an incoming noise as a wanted signal, and vice versa will not treat a wanted signal as noise.

Detecting the phase jump of a signal, is identical to detect whether the signal is at the expected data rate. In fact, at the same time, the PJD will also detect the FSK deviation and see if it is valid, as well as to see if the SNR is over 7 dB. According to detect result of the data rate and the Deviation as well as SNR, if it is detected as a reliable signal, it outputs logic 1, otherwise outputs logic 0. The output can be used as a source of the RSSI VLD interrupt, or the receive time extending condition in thesuper low power (SLP) mode. In direct data mode, by setting the DOUT_MUTE register bit to 1, the PJD can mute the FSK demodulated data output while there is not wanted signal received.

The PJD technique is similar to the traditional carrier sense technique, but more reliable. While users combine the RSSI detection and PJD technique, they can precisely identify the status of the current channel.

4.9 Clock Data Recovery（CDR）

The basic task of a CDR system is to recover the clock signal that is synchronized with the symbol rate while receiving the data. Not only for decoding inside the chip, but also for outputting the synchronized clock to GPIO for users to sample the data. So CDR's task is simple and important. If the recovered clock frequency is in error with the actual symbol rate, it will cause data acquisition errors at the time of reception.

CMT2380F29 supports 3 CDR systems for different requirements:

- **COUNTING system** – The system is designed for the symbol rates to be more accurate. If the symbol rate is100% aligned, the unlimited length of 0 can be received continuously without error.
- **TRACING system** – The system is designed to correct the symbol rate error. It has the tracking function. It can automatically detect the symbol rate transmitted byTX, and adjust quickly the local symbol rate of RX at the

sametime, so as to minimize the error between them. The system can withstand up to 15.6% symbol rate error. Other similar products in the industry cannot reach this level.

- **MANCHESTER system**–This system evolves from the COUNTING system. The basic feature is the same. The only difference is that the system is specially designed for Manchester codec. Special processing can be done when the TX symbol rate has unexpected changes

4.10 Fast Frequency Hopping

The mechanism of fast frequency hopping is, based on the frequency configured on the RFPDFK, for instance 433.92 MHz, during applications the MCU can simply change 1 or 2 registers to quickly switch to another frequency points. This simplifies way of changing RX or TX frequency in multiple channels application.

$$\mathbf{FREQ = Base\ frequency\ point + 2.5\ kHz \times FH\_OFFSET<7:0> \times FH\_CHANNEL<7:0>}$$

In general, users can configure FH_OFFSET<7:0>during the chip initialization process. And then in the application, users can switch the channel by switching FH_CHANNEL<7:0>.

If parameters of AFC have to be re-configured in some particular situation when it is under the fast frequency hopping in receiving mode, please refer to AN197-CMT2300A-CMT2119B-CMT2219B fast frequency hopping and CMT2300A-CMT2219B frequency hopping calculation tool for more details.

4.11 Chip Operation

4.11.1 SPI Interface

The chip communicates with the outside through the 4-wire SPI interface (FCSB、CSB 、SDA、SCLK).The CSB is the active-low chip select signal for accessing to the registers. The FCSB is the active-low select signal for accessing to the FIFO.They cannot be set to low at the same time. The SCLK is the serial clock. Its highest speed is 5MHz.The chip itself and the external MCU send the data at the falling edge of SCLK and capture the data at the rising edge of SCLK. The SDIO is a bidirectional pin for input and output data. The address and data are transferred starting from the MSB.

When accessing to the register, CSB is pulled low. A R/W bit is sent first, followed by a 7-bit register address. After the external MCU pulls down the CSB, it must wait for at least half a SCLK cycle, and then send the R/W bit. After the MCU sends out the last falling edge of SCLK, it must wait for at least half a SCLK cycle, and then pull the CSB high.

To be noticed, when reading a register, both the controller and the transceiver will switch the IO (SDA) port between address 0 and data 7. In this case, the SDA switches the I/O port from input to output, and the controller switches the corresponding I/O port from output to input. Noted the dotted line in the middle. It is strongly recommended that the controller switch the I/O port to input before sending out the falling edge of the SCLK. The transceiver does not switch the IO to output until it sees the falling edge. This avoids the electrical conflict caused by both setting SDA as output.

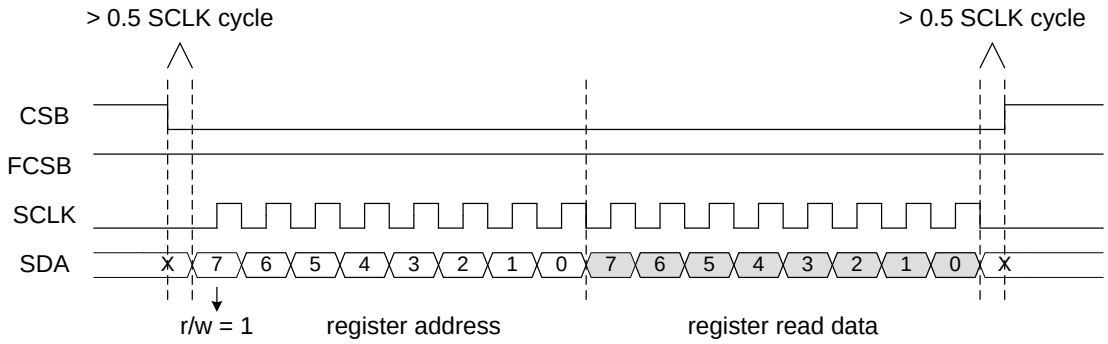


Figure 4-5. SPI Read Register Timing

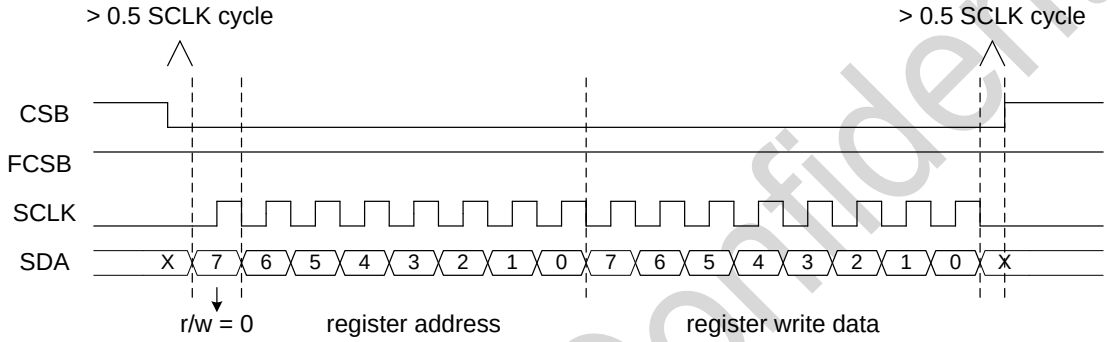


Figure 4-6. SPI Write Register Timing

4.11.2 FIFO Interface

CMT2380F29 provides two separated 32-byte FIFO by defaul for RX and TX respectively. RX FIFO is used to store the received data in RX mode and TX FIFO is used to store the transmitting data in TX mode. Users can also set FIFO_MARGE_EN to1 to merge the two separated FIFO into one 64-byte FIFO. It can be used both underTX and RX. By configuring the FIFO_RX_TX_SEL to indicate whether it is currently used as TX FIFO or RX FIFO. When the two FIFO are not merged, users can fill in the next time 32-byte TX FIFO while the 32-byte RX FIFO is filled in the RX mode to save operation time.

The FIFO can be accessed via the SPI interface. The user can clear the FIFO by setting FIFO_CLR_TX or FIFO_CLR_RX to 1. Also, the user can re-send the old data in the TX FIFO by setting FIFO_RESTORE to 1, without the need of re-filling the data.

When the MCU accesses to the FIFO, the user must first configure a few registers to set up the FIFO read/write mode, as well as some other working mode. The details are introduced in “AN143-CMTT2300A FIFO and Data Packet Usage Guideline”. Here is the read-write timing diagram. Noted that there is a slight difference in the control of the FCSB for accessing to the FIFO and the control of the CSB for accessing to the register. When the MCU starts to access to the FIFO, FCSB must be pulled down 1-clock cycle at first, and then send the rising edge of SCL. After the last falling edge of SCL is sent, the MCU must wait at least 2 us to pull up the FCSB. Between the adjacent read/write operations, the FCSB must be pulled high for 4us at least. When writing the FIFO, the first bit data must be ready 0.5 clock cycles before sending the first rising edge of SCL.

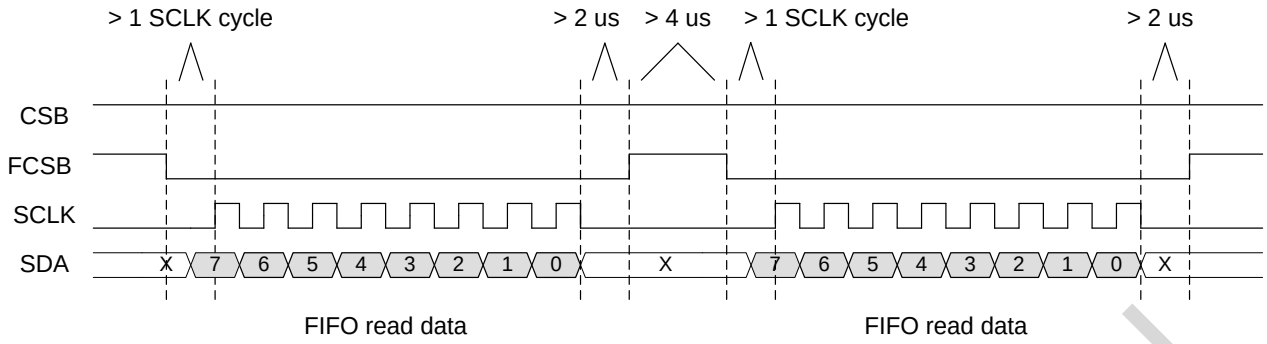


Figure 4-7. SPI Read FIFO Timing

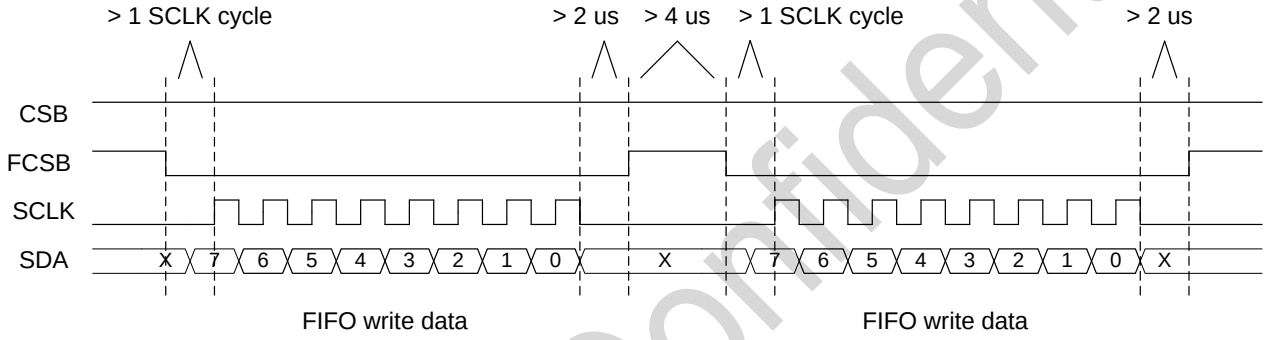


Figure 4-8. SPI Write Register Timing

The transceiver provides several FIFO related interrupt sources as auxillary tool for efficient chip operation. The related FIFO interrupt sequence is shown as followed.

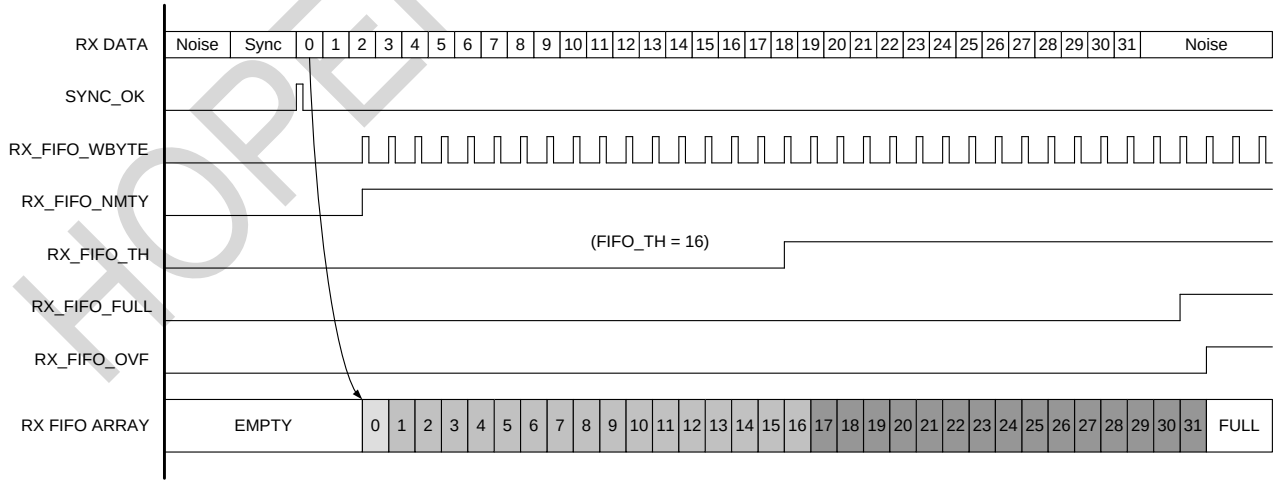


Figure 4-9. Transceiver RX FIFO Interrupt Sequence Diagram

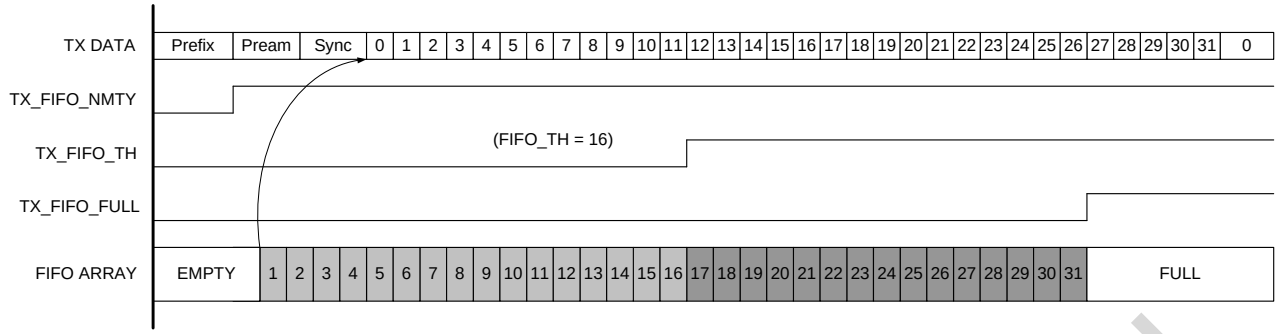


Figure 4-10. Transceiver TX FIFO Interrupt Sequence Diagram

4.11.3 Transceiver working status, timing and power consumption

- Startup time

After the transceiver is powered on RF-VDD, it usually needs to wait for about 1ms until POR released. After the RELEASE of POR, the crystal will also start. The startup time is assumed to be N ms, which depends on the characteristics of the crystal itself. After startup, it is necessary to wait for the crystal to stabilize the system before starting to work. The default stability time is 2.48 ms, which can be written to XTAL_STB_TIME <2:0>; After modification, the chip will stay in IDLE state until the crystal is stable. After the crystal is stable, the chip will leave IDLE and start to do the calibration of each module. After the calibration, the chip will stay in SLEEP, waiting for the user to initialize the chip. The chip returns to IDLE and starts the power-on process again

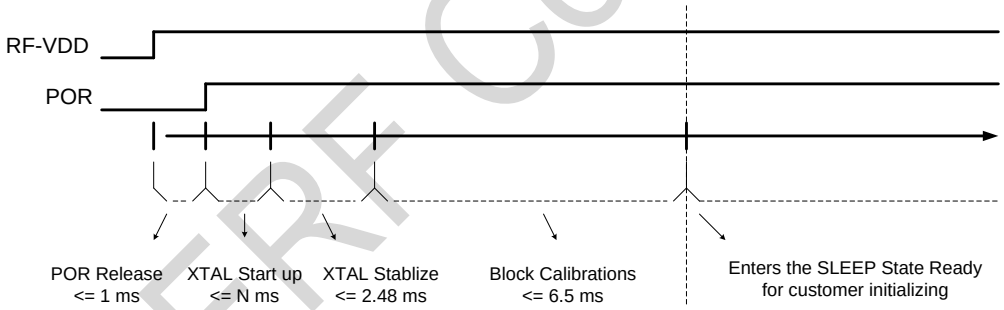


Figure 4-11. Power On Timing

The chip enters SLEEP state after calibration. And then, the MCU can control the chip to switch to different operation states through setting the register CHIP_MODE_SWT<7:0>.

- Operation State

CMT2380F29 has 7 operation states: IDLE, SLEEP, STBY, RFS, RX, TFS and TX, as shown below：

Table 4-1. Transceiver State and Corresponding Active Module

State	Binary code	Switch command	Active module	Optional module
IDLE	0000	soft_rst	SPI, POR	None
SLEEP	0001	go_sleep	SPI, POR, FIFO	LFOSC, Sleep Timer
STBY	0010	go_stby	SPI, POR, XTAL, FIFO	CLKO
RFS	0011	go_rfs	SPI, POR, XTAL, PLL, FIFO	CLKO
TFS	0100	go_tfs	SPI, POR, XTAL, PLL, FIFO	CLKO
RX	0101	go_rx	SPI, POR, XTAL, PLL, LNA+MIXER+IF, FIFO	CLKO, RX Timer
TX	0110	go_tx	SPI, POR, XTAL, PLL, PA, FIFO	CLKO

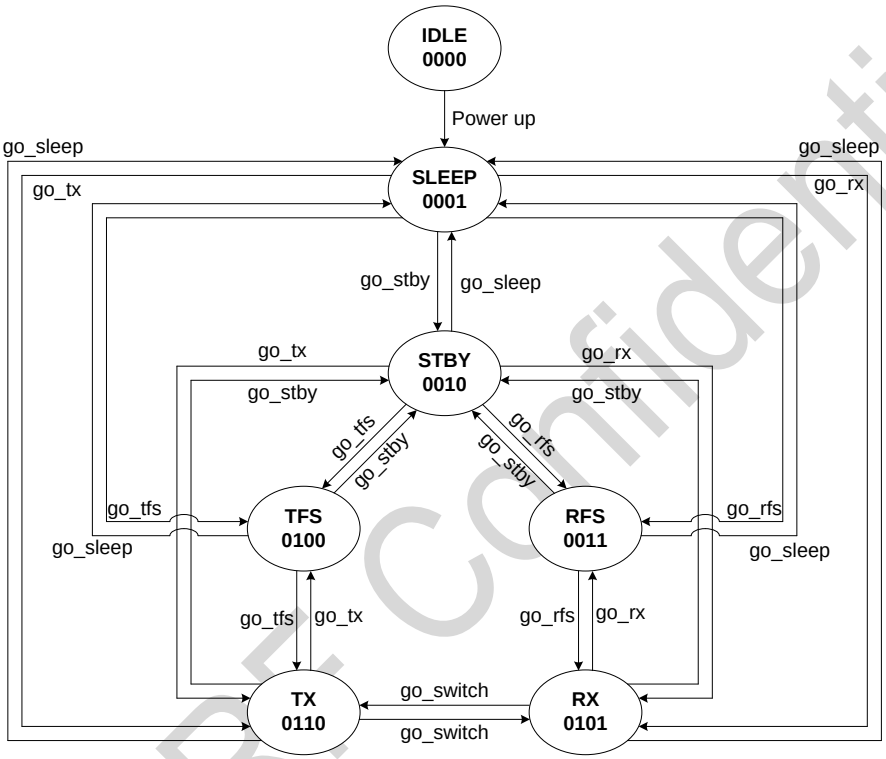


Figure 4-12. State Switch Diagram

➢ SLEEP State

The chip power consumption is the lowest in SLEEP state, and almost all the modules are turned off. SPI is open, the registers of the configuration bank and control bank 1 will be saved, and the contents filled in the FIFO before will remain unchanged. However, the user cannot operate the FIFO and cannot change the contents of the register. If the user opens the wake-up function, the LFOSC and the sleep counter will turn on and start working. The time required to switch from IDLE to SLEEP is the power up time. Switch from other state to SLEEP will be completed immediately.

➢ STBY State

In STBY state, the LDO of the digital circuit will be turned on as the crystal is on and the current will be slightly increased, the FIFO can be operated at the same time. User can choose whether to output CLKO (system clock) to PIN or not. Because the crystal and LDO is turned on, the time switching from the STBY to transmitting or receiving will be relatively short. Switching from SLEEP to STBY will be completed after the crystal is turned on and settled while switching from other state to STBY will be completed immediately.

➢ **RFS State**

RFS is a transition state before switching to RX. Except that the receiver RF module is off, the other modules are turned on, and the current will be larger than STBY. Because PLL has been locked in the RX frequency, RFS cannot switch to TX. Switching from STBY to RFS requires time of 350 us after PLL calibration and stability. Switching from SLEEP to RFS needs to add the crystal start-up and stability time. Switching from other state to RFS will be completed immediately.

➢ **TFS State**

TFS is a transition state before switching to TX. Except that the receiver RF module is off, the other modules are turned on, and the current will be larger than STBY. Because PLL has been locked in the TX frequency, TFS cannot switch to RX. Switching from STBY to TFS requires 350 us after PLL calibration and stability. Switching from SLEEP to TFS needs to add the crystal start-up and stability time. Switching from other state to TFS will be completed immediately.

➢ **RX State**

All modules on the receiver will be opened in RX state. Switching from RFS to RX requires only 20 us. Switching from STBY to RX needs to add the PLL calibration and settled time of 350 us. Switching from SLEEP to RX needs to add the crystal start-up and settled time. TX can be quickly switched to RX by sending go_switch command. Whether the TX and RX setting frequency is the same, the user need to wait for the PLL re-calibration and settled time of 350 us to switch successfully.

➢ **TX State**

All modules on the transmitter will be opened in TX state. Switching from TFS to TX requires only 20 us. Switching from STBY to TX needs to add the PLL calibration and settled time of 350 us. Switching from SLEEP to TX needs to add the crystal start-up and settled time. RX can be quickly switched to TX by sending go_switch command. Whether the RX and TX setting frequency is the same, the user need to wait for the PLL re-calibration and settled time of 350 us to switch successfully.

4.11.4 GPIO Function and Interrupt Mapping

CMT2380F29 has 3 GPIO ports. Each GPIO can be configured as a different input or output. CMT2380F29 has 2 interrupt ports. They can be configured to different GPIO mapping output.

Table 4-2. Transceiver GPIO Function

Pin No.	Name	I/O	Function
48	GPIO1	IO	Configurable as：DOUT/DIN，INT1，INT2，DCLK (TX/RX)，RF_SWT
47	GPIO2	IO	Configurable as：INT1，INT2，DOUT/DIN，DCLK (TX/RX)，RF_SWT
9	GPIO3	IO	Configurable as：CLKO，DOUT/DIN，INT2，DCLK (TX/RX)

Below shows the Interrupt mapping in Table 4-3. INT 1 and INT 2 mapping is the same. Take INT 1 as an example.

Table 4-3. Transceiver Interrupt Mapping

Name	INT1_SEL	Descriptions	Clearing methods
RX_ACTIVE	00000	Indicates the chip is entering RX and already in RX. It is 1 in PLL tuning and RX state while 0 in other states.	Auto
TX_ACTIVE	00001	Indicates the chip is entering TX and already in TX. It is 1 in PLL tuning and RX state while 0 in other states.	Auto
RSSI_VLD	00010	Indicates whether the RSSI is active.	Auto
PREAM_OK	00011	Indicates that the Preamble is received successfully.	by MCU
SYNC_OK	00100	Indicates that the Sync Word is received successfully.	by MCU
NODE_OK	00101	Indicates that the Node ID is received successfully.	by MCU
CRC_OK	00110	Indicates that the CRC for the current packet is correct.	by MCU
PKT_OK	00111	Indicates that a packet has been received.	by MCU
SL_TMO	01000	Indicates that the SLEEP counter timed out.	by MCU
RX_TMO	01001	Indicates that the RX counter timed out.	by MCU
TX_DONE	01010	Indicates that the TX operation is completed.	by MCU
RX_FIFO_NMTY	01011	Indicates that the RX FIFO is not empty.	Auto
RX_FIFO_TH	01100	Indicates the number of unread bytes of the RX FIFO is over FIFO TH	Auto
RX_FIFO_FULL	01101	Indicates RX FIFO is full.	Auto
RX_FIFO_WBYTE	01110	Indicates each time a byte is written to the RX FIFO.It is a pulse.	Auto
RX_FIFO_OVF	01111	Indicates RX FIFO is overflow	Auto
TX_FIFO_NMTY	10000	Indicates that TX FIFO is not empty	Auto
TX_FIFO_TH	10001	Indicates the number of unread bytes of the TX FIFO is over FIFOTH.	Auto
TX_FIFO_FULL	10010	Indicates TX FIFO is full.	Auto
STATE_IS_STBY	10011	Indicates that the current state is STBY.	Auto
STATE_IS_FS	10100	Indicates that the current state is RFS or TFS.	Auto
STATE_IS_RX	10101	Indicates that the current state is RX.	Auto
STATE_IS_TX	10110	Indicates that the current state is TX.	Auto
LBD	10111	Indicates that low battery is detected (VDD is lower than TH)	Auto
TRX_ACTIVE	11000	Indicates the chip is entering TX or RX and is already in TX or RX. It is 1 in PLL tuning, TX or RX state while it is 0 in the otherstates.	Auto
PKT_DONE	11001	Indicates that the current packet has been received, covering 4 possible different situations. 1. The packet is received completely and correctly. 2. Manchester decoding error. Decoder is automatically reset. 3. NODE ID receiving error. Decoder is automatically reset. Signal collision occurred. Decoder is not reset, waiting for MCU to response.	by MCU

By default, interrupt is active high (logic1 is valid). Users can set the INT_POLAR register bit to 1 to make all interrupts active low (logic 0 is valid). Taking INT 1 as an example, the control and sources selection of all the available interrupts is shown below. The control and mapping of INT 1 and INT 2 are the same.

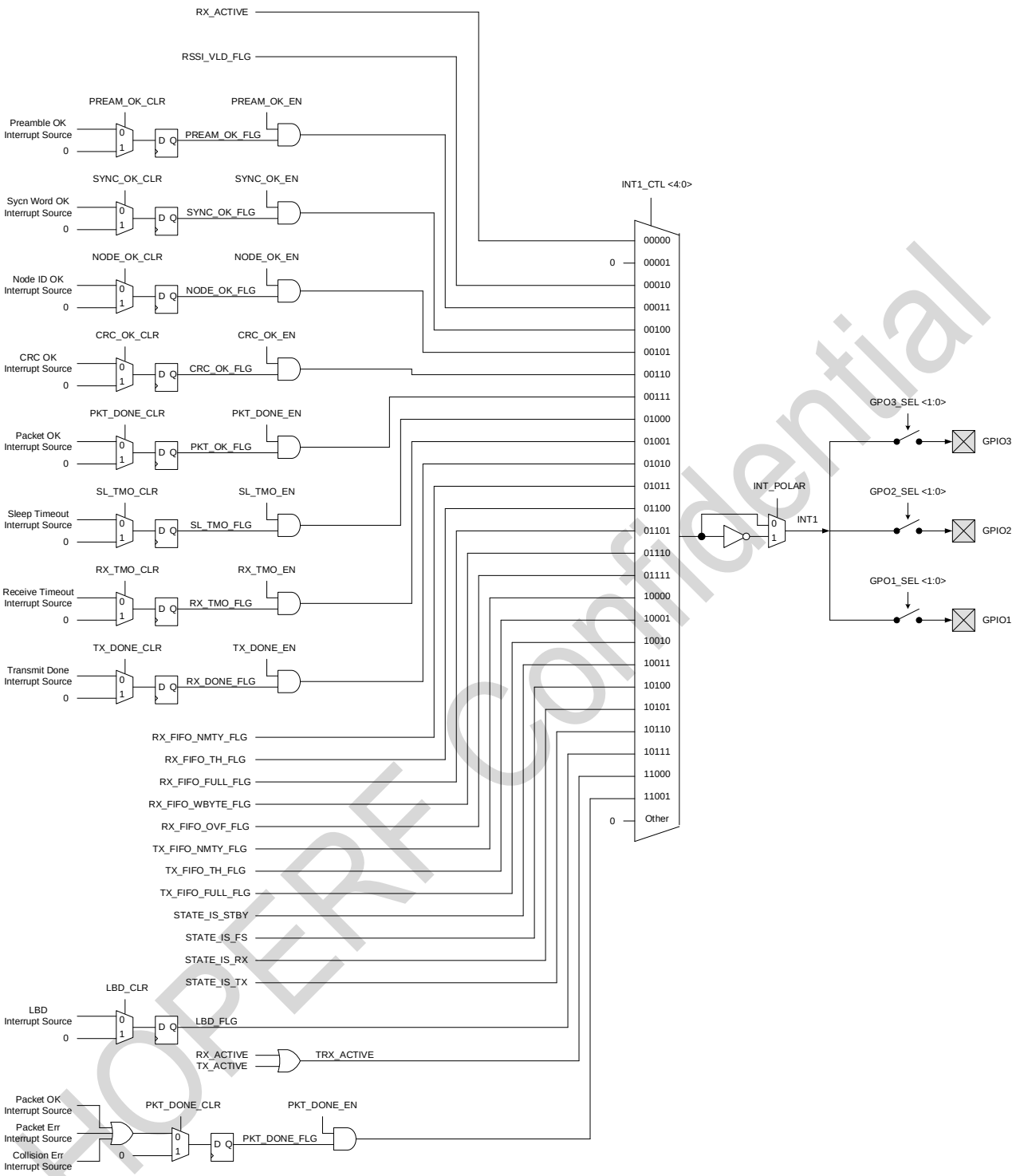


Figure 4-13. CMT2380F92 INT1 Interrupt Mapping

5 Function Description

5.1 Memeory

CMT2380F29 includes embedded encrypted flash memory (Flash) and embedded SRAM, Figure 5-1 below shows the memory address map.

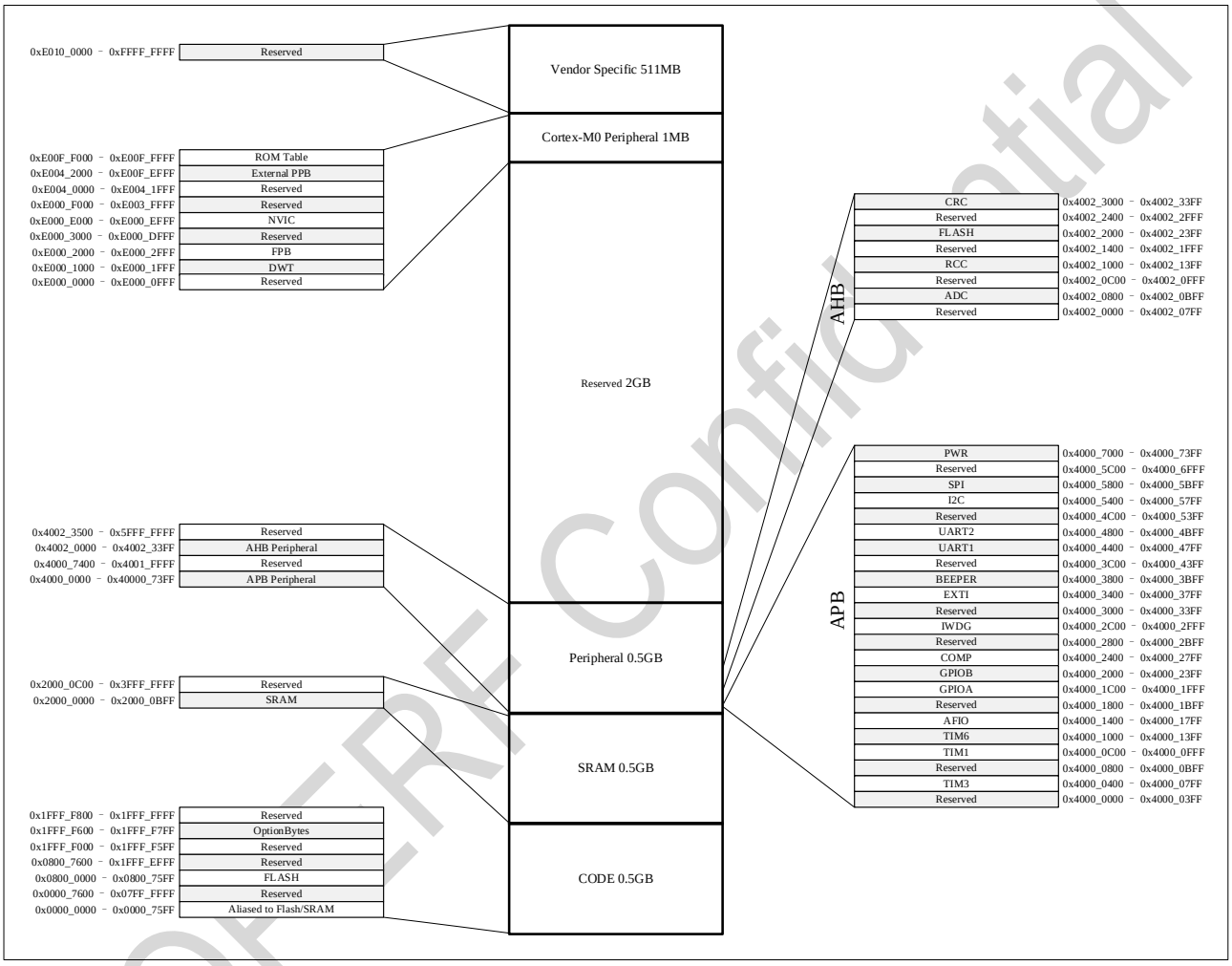


Figure 5-1. Memory Address Map

5.1.1 Embedded Flash Memory

The chip integrates 29.5K bytes of embedded flash memory (FLASH) for storing programs and data. The page size is 512 byte and supports page erase, word write, word read, half-word read, and byte read operations.

5.1.2 Embeded SRAM

Up to 3K bytes of built-in SRAM is integrated on-chip, and data can be maintained in the STOP mode

5.1.3 Nested Vectored Interrupt Controller（NVIC）

The Nested Vectored Interrupt Controller (NVIC) is closely connected to the interface of the processor core, which can realize

low-latency interrupt processing and efficiently handle late-arriving interrupts. The nested vectored interrupt controller manages interrupts including kernel exceptions.

- 16 maskable interrupt channels(not including 16 Cortex®-M0 interrupt lines）；
- 4 programmable priority levels (using 2-bit interrupt priority levels)；
- Low-latency exception and interrupt handling；
- Power management control；
- Realization of system control register；

5.2 Extended Interrupt / Event Controller (EXTI)

The extended interrupt/event controller includes 20 edge detection circuits that generate interrupts/event triggers. Each input line can be independently configured as an event or interrupt, as well as three trigger types of rising edge, falling edge or both edges, and can also be independently shielded. The suspend register holds the interrupt request of the status line, and the corresponding bit of the suspend register can be cleared by writing '1'.

5.3 Clock System

The clock of the device includes internal high-speed RC oscillator HSI (48MHz or 40MHz), internal low-speed clock LSI (32 KHz).

The SYSCLK can be triggered by the HSI osillator clock source.

32 KHz low-speed internal RC，which is used as the secondary clock source, can select the IWDG and TIM6 (wakeup the system from STOP mode) through program.

Multiple pre-dividers can be used to configure the frequencies of AHB and APB. The maximum frequency of AHB and APB is 48MHz.

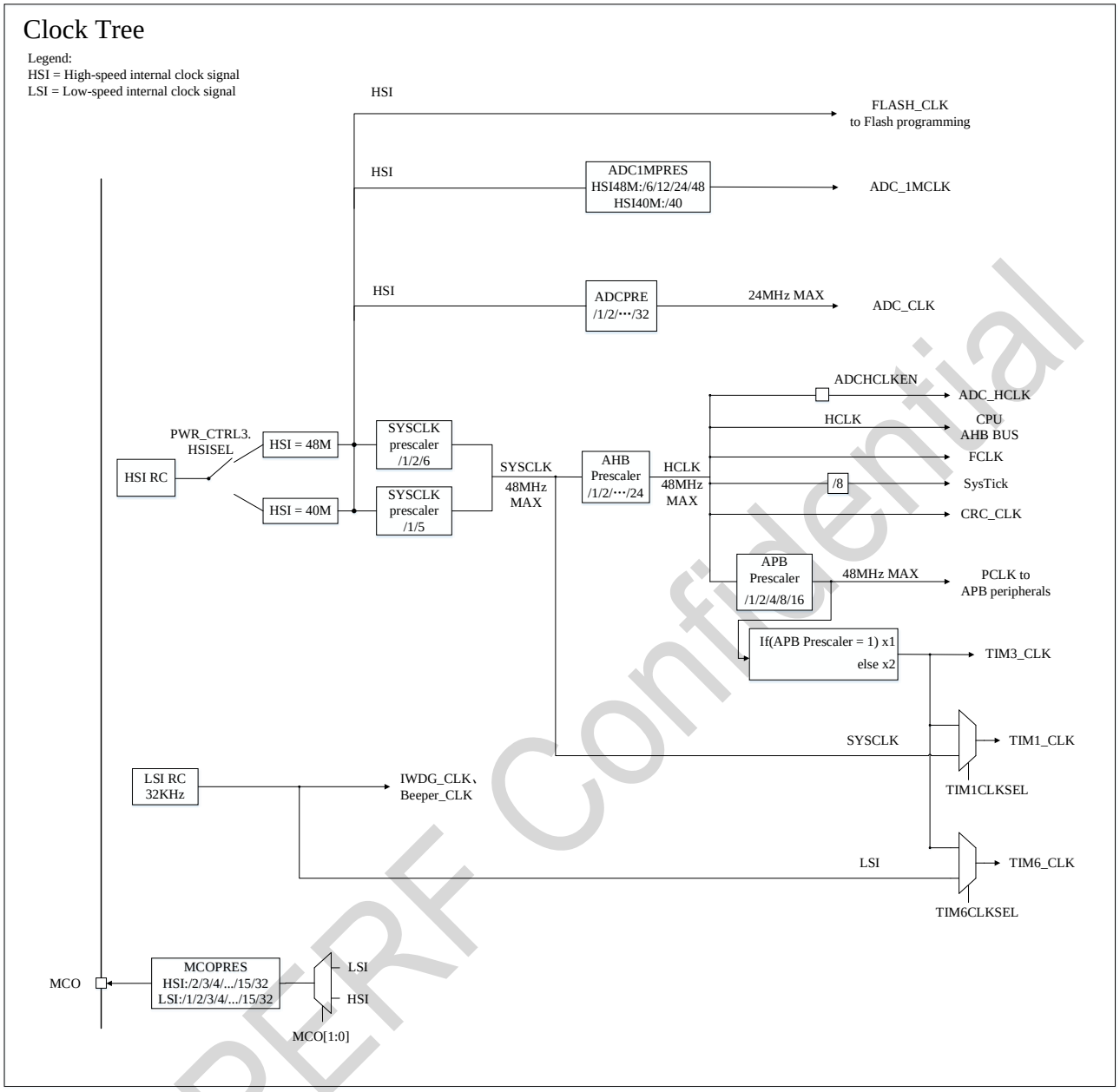


Figure 5-2. Clock Tree

5.4 Boot Modes

The FLASH Memory start at 0x08000000.

5.5 Power Supply Scheme

- VDD area：The voltage input range is 2.0 V~3.6 V，which mainly provides power input for Main Regulator, IO and clock reset system.
- VDDD area：The voltage regulator supplies power for CPU, AHB, APB, SRAM, FLASH and most of the digital peripheral interfaces.
- PWR is the power control module of the entire device, its main function is to control MCU to enter into different power

modes and can be awakened by other events or interrupts. CMT2380F29 supports RUN, STOP and PD modes.

5.6 Programmable Voltage Monitor

The power-on reset (POR) and power-down reset (PDR) circuits are integrated internally. This part of the circuit is always in working condition to ensure that the system works normally when the power supply voltage exceeds 2.0 V. When V_{DD} is lower than the threshold ($V_{POR/PDR}$), the device remains in the reset state. The device has a programmable voltage monitor (PVD), which monitors the V_{DD} power supply and compares it with the threshold V_{PVD}. When V_{DD} is lower or higher than the threshold V_{PVD}, it will generate an interrupt. The PVD function is turned on by software.

For the reference values of $V_{POR/PDR}$ and V_{PVD}, please refer to the table for Embedded Reset and Power Control Module Features

5.7 Low Power Mode

CMT2380F29 is in operation mode after system reset or power-on reset. When the CPU does not need to run (for example, waiting for external events）, users can choose to enter low-power mode to save power. The low power mode is selected by the user among low power consumption, short startup time, and available wake sources.

The low power mode features are shown as followed：

- STOP mode（most of the clocks are turned off, the voltage regulator is still running in low power consumption mode）
- PD mode（VDDD power-down mode，VDD hold，2 WAKEUP IO and NRST can be wake up）

  Besides, low power consumption can be achieved in RUN mode as followed:

  - Reduce the system clock frequency
  - Turn off the unused peripheral clocks on the APB and AHB buses
  - Configure PWR_CTRL4.STBFLH in RUN mode and allow FLASH to enter deep standby mode;

5.8 Timer and Watch Dog

CMT2380F29 supports 1 advanced-control timers, 1 general-purpose timer, 1 basic timer and 1 watchdog timers as well as 1 system tick timer.

The following table compares the functions of advanced-control timers, general-purpose timers and basic timers:

Table 5-1. Timer Function Comparison

Timer	Counter resolution	Counter type	Prescaler	Capture/ Compare channel	Complementary output
TIM1	16 bits	Up Down Up/Down	Any integer between 1~65536	4	support
TIM3	16 bits	Up Down Up/Down	Any integer between 1~65536	2	unsupport

Timer	Counter resolution	Counter type	Prescaler	Capture/ Compare channel	Complementary output
TIM6	16 bits	Up	Any integer between 1~65536	0	unsupport

5.8.1 Basic Timer TIM6

The basic timer (TIM6) contains a 16-bit auto-load counter, driven by a programmable prescaler, which can wakeup the system from low power mode.

The main functions of the basic timer are as follows:

- 16 bit automatic reload accumulating counter；
- 16 bit programmable (can be modified in real time) prescaler，used to divide the input clock by coefficient between 1 and 65536；
- Support STOP mode wakeup: STOP mode can be wakeup by updating interrupts while the clock source is configured as LSI.

5.8.2 General Purpose Timer TIM3

General purpose timer (TIM3) is mainly applied in the following situations: count the input signal, measure the pulse width of the input signal and generate the output waveform.

The main functions of the general-purpose timer include：

- 16 bit up,down, up/down automatic loading counter；
- 16 bit programmable (can be modified in real time) prescaler, the frequncy division coefficient of the counter clock frequncy is any integer between 1～65536；
- 2 independent channels
- Channel operating mode：PWM output，output comparision，single pulse mode output, input capture
- Interrupt is generated when the following events occur：
  - Update event
  - Triggered event
  - Input capture
  - Output comparision
- Control timer through external signals
- Multiple timers are connected together internally to achieve timer synchronization or linking
- Supports capture of internal comparator output signals

5.8.3 Advanced Control Timer TIM1

Advanced control timer (TIM1) is applied in the following occasions: to count the input signal, measure the pulse width of the input signal and generate the output waveform.

Advanced timer includes function of complementary output, dead zone insertion, and braking. It is suitable for motor control.

The main functions of the advanced timer include:

- 16-bit up, down, up/down automatic loading counter

- 16-bit programmable (can be modified in real time) prescaler, the frequency division coefficient of the counter clock frequency is any value between 1 and 65536

◆ Programmable repeat counter

◆ Up to 5 channels

◆ Up to 4 independent channels:

- Input capture
- Output comparision
- PWM generation (edge or center alignment mode)
- Single pulse mode output

Interrupt is generated when the following events occur:

- Update event
- Triggered event
- Input capture
- Output comparision
- Break signal input

Dead zone programmable complementary output：

◆ It is applied in channel 1,2.3 of TIM1 support

◆ Control the timer through external signals

◆ Multiple timers are connected together internally to achieve timer synchronization or linking

◆ TIM1_CC5 is applied in comparator blanking

5.8.4 Systick

This timer is specific for real-time operating system and can also be used as a standard decrement counter.

It has the following characteristics:

◆ 24-bit decrement counter

◆ Automatic reload function

◆ A maskable system interrupt can be generated when the counter is 0

◆ Programmable clock source

5.8.5 Watchdog Timer WDG

It supports one Independent Watchdog (IWDG) and one Window Watchdog (WWDG). Two watchdogs provide increased security, timing accuracy and flexibility in use.

◆ **Independent Watchdog（IWDG）**

The independent watchdog is based on a 12-bit decline counter and a 3-bit prescaler, driven by an independent low-speed RC oscillator that remains effective in the event of a master clock failure and operates in STOP mode. Once activated, IWDG generates a reset when the counter counts to 0x000 if the dog is not fed within the set time (clearing the watchdog counter). It can be used to reset the entire system in the event of an application problem, or as a free timer to provide timeout management for the application. The option byte can be configured to be software or hardware enabled watchdog. Reset and low power

wake-up are available.

5.9 I²C Bus Interface

It has one independent I²C bus interface that provide multi-host functionality to control all I²C bus specific timing, protocol, mediation, and timing. It can support multiple communication rate modes (up to 1MHz). The I²C module has a variety of uses, including CRC code generation and verification.

The main functions of I²C interface are described as follows:

- The module can be used as a master device or a slave device;
- I²C master device function：
  - Generate clock;
  - Generate start and stop signals;
- I²C slave device function:
  - Progranmable address detection;
  - The I2C interface supports 7 bit or 10 bit addressing and supports dual slave address response in 7 bit slave mode;
  - Stop bit detection;
- Generate and detect 7 bit /10 bit addresses and broadcast calls;
- Support diferent communication speeds：
  - Standard speed (up to 100 kHz);
  - Fast (up to 400 kHz)；
  - Fast + (up to 1 MHz)；
- Status flag:
  - Transmitter / receiver mode falg;
  - Byte end flag;
  - I2C bus busy sign;
- Error flag:
  - Arbitration lost in master mode;
  - Response（ACK）error after address/data transmission;
  - Misaligned start or stop conditions detected;
  - Prohibit overflowing or underflowing when elongating the clock function;
- 2 interrupt vectors:
  - Event interrupt;
  - Error interrupt;
- Optional elongated clock feature;
- Generate or verify configurable PEC (packet error detection):
  - The PEC value can be sent as the last byte in transmission mode
  - It is used for PEC error check of the last received byte

5.10 Universal Asynchronous Receiver Transmitter（UART）

CMT2380F29 integrates 2 universal asynchronous transceivers (UART1/ UART2).

UART1 and UART2 provide asynchronous communication, support for multi-processor communication mode, single-wire half-duplex communication mode.

The main features of UART are as follows:

- Full-duplex, asynchronous communication;
- NRZ standard format;
- Single-wire half-duplex communication；
- Baud rate configurable
- Programmbale data word length (8 or 9 bits)
- Supporting 1 or 2 stop bits
- Supports hardware generation and bits check
- Supports Multi-processor communication: if the address does not match, then into silent mode
- Supports Multi-processor communication: wake up from silent mode (Detect by idle bus or address flag detection)
- Supports Multi-error detection: overflow error, frame error, noise error, check error.
- 8 interrupt request:
  - Tx data register empty
  - Tx complete
  - Receive data register full
  - Bus detected as idle
  - Overflow error
  - Noise error
  - Frame error
  - Check erro
- Mode configuration

USART modes	UART1	UART2
Asynchronous mode	√	√
Multiprocessor communication	√	√
Half duplex (single wire mode)	√	√

5.11 Serial Perigheral Interface（SPI）

Support 1 SPI interface, SPI allows the chip to communicate with external devices in half/full duplex, synchronous, serial mode. This interface can be configured to be in master mode and provide a communication clock (SCK) for external slave devices. The interface can also work in a multi-master configuration. It can be used for a variety of purposes, including dual wire simplex synchronous transmission using a two-way data line.

The main functions of the SPI interface are as follows:

- Full and half duplex synchronous transmission
- 8 / 16 bit transmission frame format selection;
- Support master mode or slave mode
- Support multi-master mode
- Programmable data order
- Hardware or software chip selection management
- Configurable clock polarity and clock phase

5.12 General Purpose Input/Output（GPIO）

GPIO (General Purpose Input/Output) stands for Generic I/O.The chip supports up to 18 GPIOs and is divided into 2 groups (GPIOA / GPIOB), group A has 16 ports per group, group B has 2 ports. Users can configure them flexibly according to their needs. Each GPIO pin can be independently configured as an output, input, or multiplexed peripheral function port. Except for analog input pins, all other GPIO pins have high current flow capability.

The main characteristics of GPIO are described as follows:

- Input floated
- Input pull-up
- Input pull down
- Analog function
- Open drain output and up/down can be configured
- Push-pull output and up/down configurable
- Push-pull multiplexing function and up/down configurable

- Separate bit setting or bit clearing
- All IO support external interrupt functionality
- All IO support low-power mode wake-up, with rising or falling edges configurable
  - 18 EXITs can be used for SLEEP or STOP mode wake up, and all I/O can be reused as EXTI
  - 3 wake-up IO of NRST(PA 0) /PA1/ PA 2 can be used for PD mode wake-up, I/O filtering time is 1us maximum
- Supports software remapping the I/O reusing function
- Support GPIO locking mechanism, reset mode to clear the locked state
- Each I/O port bit can be programmed arbitrarily, but the I/O port register must be accessed as a 32-bit word (16-bit half-word or 8-bit byte access is not allowed).

5.13 Analog / Digital Converter（ADC）

12-bit ADC is a high-speed successive approximation analog-to-digital converter. It has up to 10 channels and can measure 9 external and 1 internal signal sources. The A/D conversion of each channel can be executed in single, continuous, scanning mode. The ADC result can be left-aligned or right-aligned stored in the 16-bit data register; The analog watchdog can detect if the input voltage is within a user-defined high/low threshold and ADC input clock must not exceed 24 MHz.

The main characteristics of ADC are described as follows:

- Support 1 ADC, single-ended input, can measure 9 external and 1 internal signal sources
- Support 12-bit resolution, the highest sampling rate is 1 MSPS
- ADC clock source is divided into working clock source, sampling clock source and timing clock source
  - HSI can be configured as a working clock source of ADC_CLK, up to 24 MHz
  - HSI can be configured as the timing clock source of ADC_IMCLK, it is used as internal timing functions, and the frequency must be configured to 1 MHz.
- Support timer trigger ADC sampling
- Interrupts are generated at the end of conversion, and the occurrence of analog watchdog events
- Single and continuous conversion mode
- Auto mode supports up to 5 channels, each channel owns an independent data result register buffer.
- Sampling interval can be programmed separately per channel
- Supports for external trigger options
- Supports for external trigger rules conversion
- ADC power supply：2.4V 到 5.5V
- ADC input range: 0 ≤ VIN ≤ VDDA

5.14 Analog Comparator（COMP）

Built-in 1 comparator, which can be used as a separate device (all ports of the comparator are led to I/O), or it can be used in combination with a timer. In motor control applications, it can be used in conjunction with the PWM output from the timer to form a cycle-by-cycle current control.

The main functions of the comparator are as follows:

- Supply voltage：2.4-5.5V
- A Comparator with subtraction, it supports for positive input voltage (500mV~VDD-200mV) minus reference voltage (300/200/100mV/0mV).
- Support filter clock
- Output polarity can be configured high and low
- Hysteresis configuration can be configured without, low, medium, high
- The comparing results can be output to the I/O port or the trigger timer for capturing events, OCREF_CLR events, braking events, and generating interrupts
- Input channel can be multi-selected I/O port
- It can be equipped with read-only or read-write, and it needs to be reset to unlock when locked

- Support blanking, the blanking source can be configured to generate Blanking
- Configurable filter window size
- Configurable filter threshold size
- Configurable sampling frequency for filtering

5.15 BEEPER

The BEEPER module supports complementary outputs and can generate periodic signals to drive external passive beeper. Used to generate prompt sound or alarm sound.

5.16 Cyclic Redundancy Check Calculation Unit（CRC）

Integrating CRC 16 functions, the cyclic redundancy check (CRC) calculation unit obtains any CRC calculation result according to a fixed generator polynomial. In many applications, CRC-based technology is used to verify the consistency of data transmission or storage.

The main characteristics of CRC are as follows:

- CRC 16：Support polynomial $X^{16}+X^{15}+X^{2}+X^{0}$
- CRC 16 calculation time： 1 AHB clock cycle (HCLK)
- The initial value of cyclic redundancy calculation can be configured

5.17 Unique Device ID（UID）

CMT2380F29 have built-in two unique device ID of different lengths, 96-bit UID (Unique device ID) and 128-bit UCID (Unique Customer ID). These two device serial numbers are stored in the system configuration block of the flash memory. The information contained in them is programmed at the factory, and is guaranteed to be unique to any micro-controller under any circumstances. User applications or external devices can be read through the CPU or SWD interface and cannot be modified.

The UID is 96 bits, usually used as a serial number or as a password. When programming the flash memory, this unique identification is combined with the software encryption and decryption algorithm to further improve the security ofthe code in the flash memory.

The UCID is 128 bits and complies with the definition of the chip serial number of HOPERF, which contains information on chip production and version.

5.18 Serial Wire SWD Debug Port（SWD）

The ARM SWD Interface is embedded in the chip.

6 Order Information

Table 6-1. CMT2380F29 Order Information

Type	Description	Package	Packet Option	Operation Condition	MOQ
CMT2380F29-EQR[1]	CMT2380F29, low power consumption Sub-1GHz RF transceiver SoC	QFN32 (5x5)	Make up with disk	2.0 to 3.6V, -40 to 85℃	3,000

Remarks:
[1]. “E” represents the extended industrial product grade，with supported temperature range from -40 to +85 ℃.
“Q” represents package type of QFN32.
“R” represents the tape and reel type with MOQ as 3,000.

For more information, please refer to official website: www.hoperf.com

Any purchasing or pricing requirements, please contact sales@hoperf.com or your local sales representatives

7 Package Outline

Package information of CMT2380F29-EQR is shown as followed.

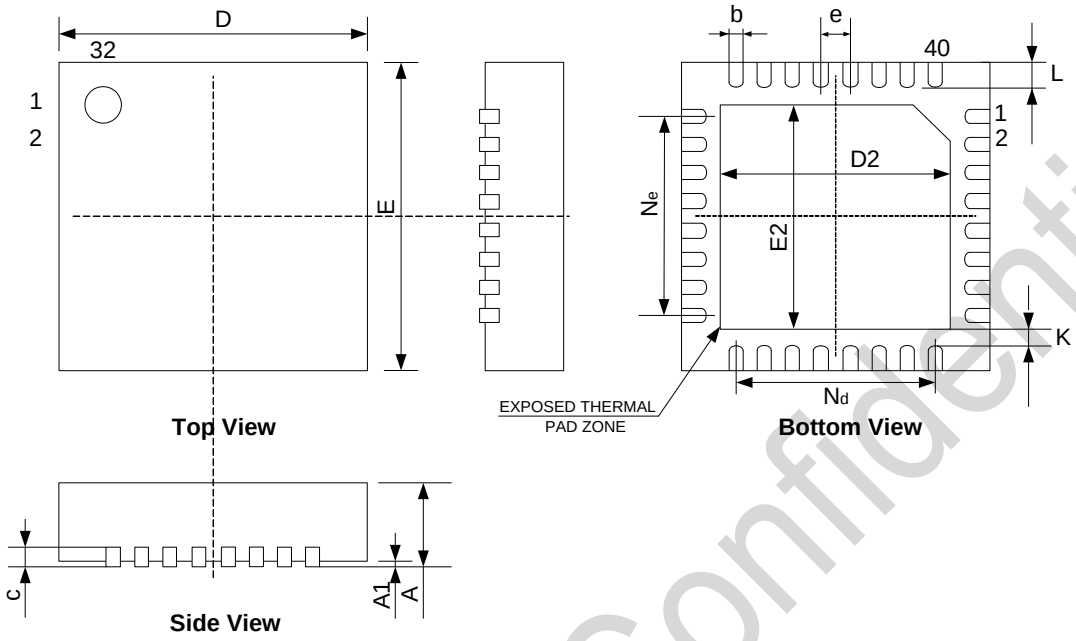


Figure 7-1. QFN32 5x5 Package

Table 7-1. QFN32 5x5 Package Size

Symbol	Size (millimeter mm)		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e	0.50 BSC		
Ne	3.50 BSC		

Symbol	Size (millimeter mm)		
	Min.	Typ.	Max.
Nd	3.50 BSC		
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.35	0.40	0.45

8 Silk Pringting Information

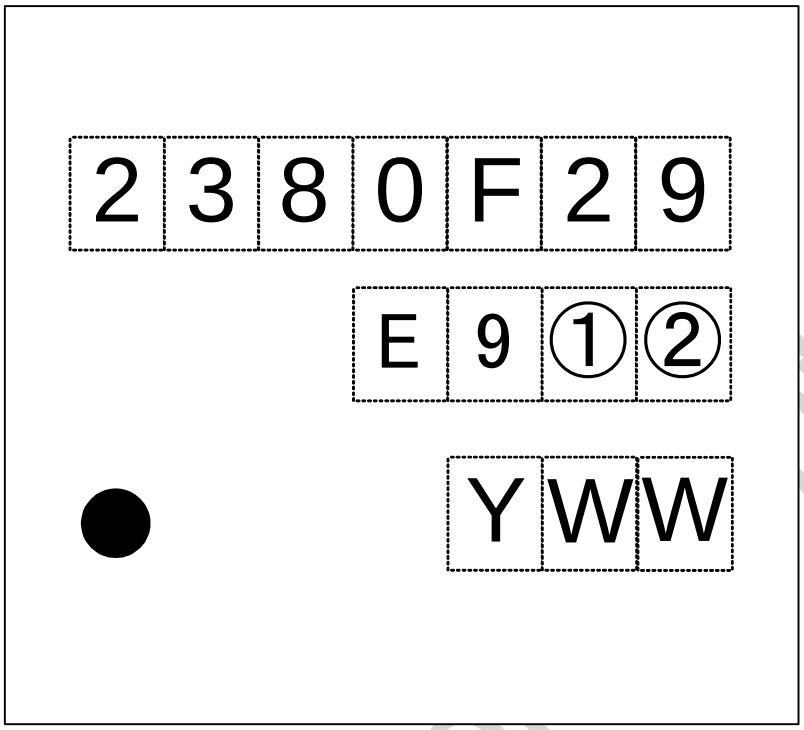


Figure 8-1. CMT2380F29 Top Mark

Table 8-1. CMT2380F29 Top Mark Description

Printing method	Laser
Pin1 marking	Circle diameter = 0.3 mm
Font size	0.5 mm, right alignment
First line silk printing	2380F29, Represents part number CMT2380F29
Second line silk printing	E9①② Internal tracking code
Third line silk printing	Date code, assigned by packaging factory, Y represents the last digit of the year and WW represents the working week

9 Relevant Documents

Table 9-1. Other Related Application Documents

Number	File Name	Description
AN141	CMT2300A Schematic Diagram and PCB Map Guide	CMT2380F29 RF match design guidelines
AN142	CMT2300A Quick User Guide	CMT2380F29 Radio frequency quick entry
AN143	CMT2300A FIFO and Packet Format User Guide	CMT2380F29 Guide to the use of RF sending and receiving messages
AN144	CMT2300A RSSI User Guide	CMT2380F29The RF RSSI using guide
AN146	CMT2300A Low Power Consumption User Guide	CMT2380F29 RF Low power design guidelines
AN147	CMT2300A Special Function User Guide	CMT2380F17RF feature function description
AN149	CMT2300ARF Parameter Configuration Guide	CMT2380F29 Description of matching parameters of RF frequency points
AN150	CMT2300ALow-voltage TXPower Compensation	CMT2380F29 Description of the RF low transmission power compensation
AN197	CMT2300A-CMT2119B-CMT2219B Fast Manual Hopping	CMT2380F29 Quick manual frequency hopping instructions
AN198	CMT2300A-CMT2119B-CMT2219B Precautions for status switch	CMT2380F29 RF state switching considerations
AN199	CMT2300A-CMT2119B-CMT2219B RF frequency calculation Guide	CMT2380F29 Description of the RF frequency calculation

10 Revision History

Table 10-1. Revision History

Version	Chapter	Modify	Date
0.1	All	Initial	2023-09-10
0.2	All	Review	2023-10-12

11 Contacts

Shenzhen Hope Microelectronics Co., Ltd.
Address: 30th floor of 8th Building, C Zone, Vanke Cloud City, Xili Sub-district, Nanshan, Shenzhen, GD, P.R. China

Tel: +86-755-82973805 / 4001-189-180
Fax: +86-755-82973550
Post Code: 518052
Sales: sales@hoperf.com
Website: www.hoperf.com