1200V N-Channel Silicon Carbide Power MOSFET

1. Applications

Asymmetrical Bridge
Converter
Inverter
Single Switch Forward
Flyback

2. Features

Low drain-source on-resistance: RDS(ON) = 40mΩ (typ.)
Easy to control Gate switching
Enhancement mode: Vth = 2 to 4 V

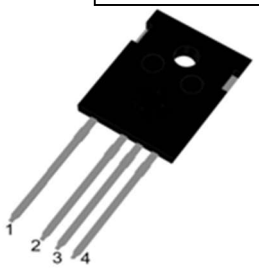
Table 1 Key Performance Parameters

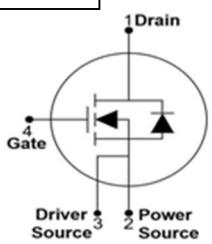
Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	1200	V
$R_{DS(on),max}$	45	mΩ
$Q_{g,typ}$	176	nC
$I_{D,pulse}$	181	A

3. Packaging and Internal Circuit

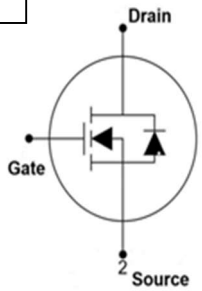
Part Name	Package	Marking
RTQ120N040	TO-247-4L	RTQ120N040
RTW120N040	TO-247-3L	RTW120N040

TO-247-4L





TO-247-3L



1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D		-	72	A	T_C=25°C
				51	A	T_C=100°C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	181	A	T_C=25°C
Gate source voltage (static)	V_{GS}	-10	-	22	V	static;
Power dissipation	P_{tot}	-	-	279	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	175	°C	
Operating junction temperature	T_j	-55	-	175	°C	

[1] Limited by $T_{j,max}$. Maximum Duty Cycle D = 0.50
[2] Pulse width t_p limited by $T_{j,max}$
[3] Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.54	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	63	°C/W	device on PCB, minimal footprint

3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	1200	-	-	V	V_{GS}=0V, I_D=100uA
Gate threshold voltage	$V_{(GS)th}$	2		4	V	V_{DS}=V_{GS}, I_D=5mA
Zero gate voltage drain current	I_{DSS}	-	-	100	uA	V_{DS}=1200V, V_{GS}=0V,
Gate-source leakage current	I_{GSS+}	-	-	100	nA	V_{GS}=22V, V_{DS}=0V
Gate-source leakage current	I_{GSS-}	-	-	-100	nA	V_{GS}=-10V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	-	40	45	mΩ	V_{GS}=18V, I_D=20A, T_j=25°C
			55			V_{GS}=18V, I_D=20A, T_j=175°C
Gate resistance (Intrinsic)	R_G	-	4.5	-	Ω	f=1MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	3640	-	pF	V_{GS}=0V, V_{DS}=600V, f=1MHz
Output capacitance	C_{oss}	-	224	-	pF	V_{GS}=0V, V_{DS}=600V, f=1MHz
Reverse transfer capacitance	C_{rss}	-	40	-	pF	V_{GS}=0V, V_{DS}=600V, f=1MHz
Turn-on delay time	$t_{d(on)}$	-	30.2	-	ns	V_{DD}=800V, V_{GS}=15V, -V_{GS} =-4V I_D=33.3A,R_G=2.5Ω; L_{Load}=500uH, T_J =25°C
Rise time	t_r	-	84.4	-	ns	
Turn-off delay time	$t_{d(off)}$	-	45.8	-	ns	
Fall time	t_f	-	16.8	-	ns	
Turn-on Switching Energy	*Eon*		1669.3		uJ	
Turn-off Switching Energy	*Eoff*		106.5		uJ	
Turn-on delay time	$t_{d(on)}$	-	17.1	-	ns	V_{DD}=800V, V_{GS}=15V, -V_{GS} =-4V I_D=33.3A,R_G=2.5Ω; L_{Load}=500uH, T_J =175°C
Rise time	t_r	-	59.2	-	ns	
Turn-off delay time	$t_{d(off)}$	-	45.7	-	ns	
Fall time	t_f	-	16	-	ns	
Turn-on Switching Energy	*Eon*		1225.2		uJ	
Turn-off Switching Energy	*Eoff*		214		uJ	

Table 6 Gate charge characteristics

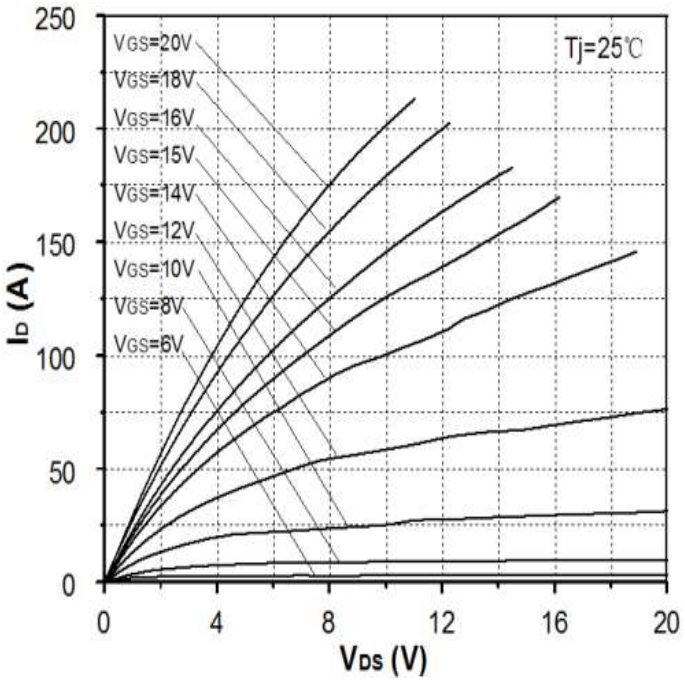
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	44	-	nC	V_{DD}=520V, I_D=10A, V_{GS}=16V
Gate to drain charge	Q_{gd}	-	58	-	nC	V_{DD}=520V, I_D=10A, V_{GS}=16V
Gate charge total	Q_g	-	176	-	nC	V_{DD}=520V, I_D=10A, V_{GS}=16V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	3.8	-	V	I_S = 20A, V_{GS} = 0V, T_j=25°C
Reverse recovery time	t_{rr}	-	57.8	-	ns	V_{DD} =800V， I_D =33.3A, +V_{GS} =+15V,-V_{GS} =-4V L_{Load}=500uH， Rg=0Ω， T_J =25°C
Reverse recovery charge	Q_{rr}	-	477.8	-	nC	
Peak reverse recovery current	I_{rrm}	-	15.84	-	A	
Reverse recovery time	t_{rr}	-	82.4	-	ns	V_{DD} =800V， I_D =33.3A, +V_{GS} =+15V,-V_{GS} =-4V L_{Load}=500uH， Rg=0Ω， T_J =175°C
Reverse recovery charge	Q_{rr}	-	1066	-	nC	
Peak reverse recovery current	I_{rrm}	-	24.92	-	A	

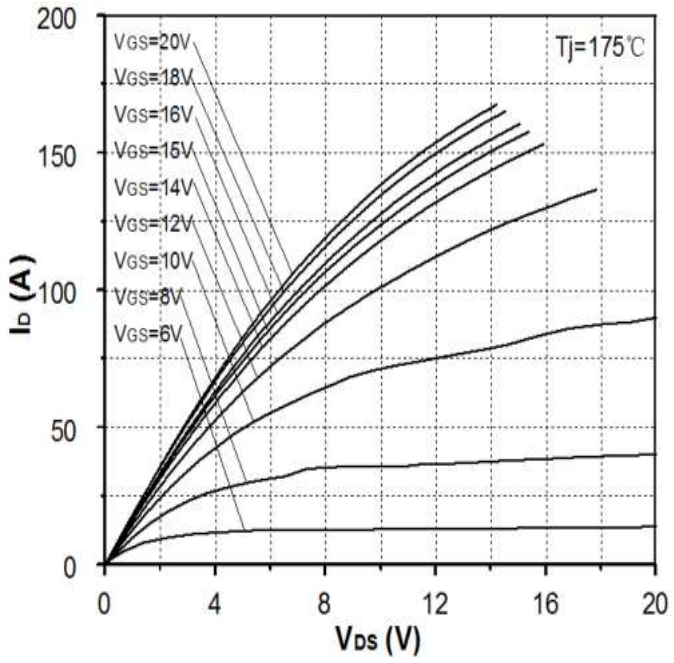
4 Electrical characteristics diagram

Diagram 1: Typ. output characteristics



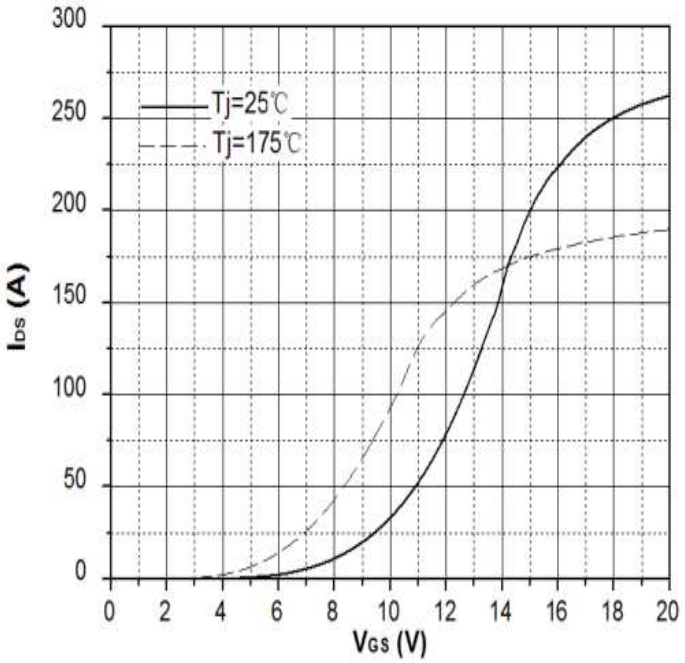
I_D=f(V_{DS});T_j=25 °C; parameter: V_{GS}

Diagram 2: Typ. output characteristics



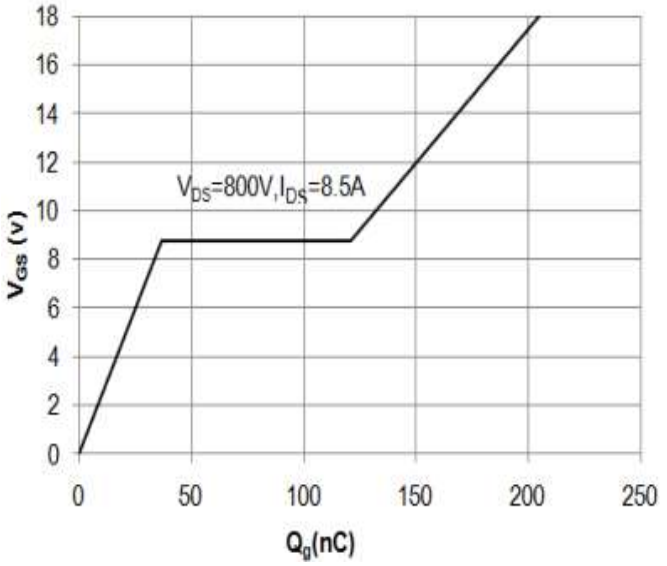
I_D=f(V_{DS});T_j=175 °C; parameter: V_{GS}

Diagram 3: Typ. transfer characteristics



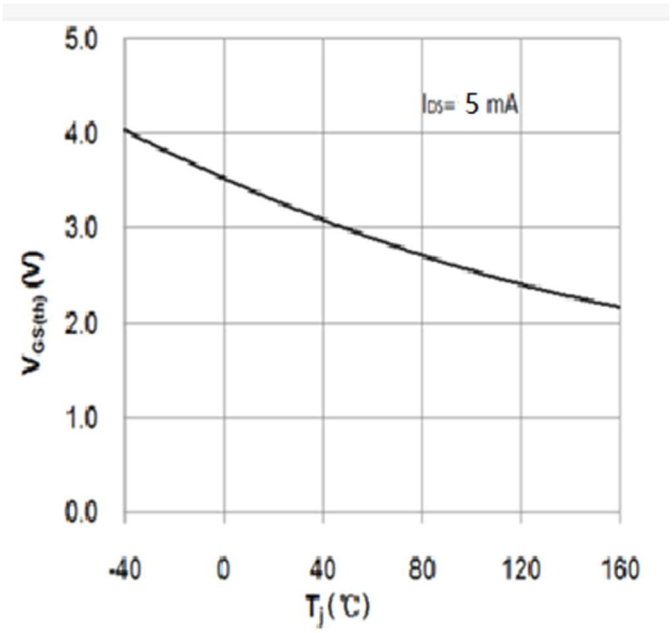
I_D=f(V_{GS}); V_{DS} =20V; parameter: T_j

Diagram 4: Typ. gate charge



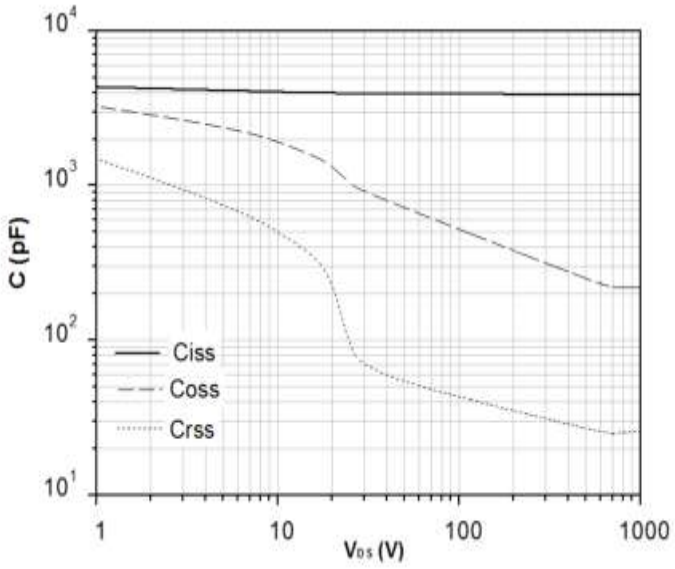
V_{GS}=f(Q_{gate});I_D=8.5A ; V_{DS} =800V; turn-on pulse

Diagram 5: Typical gate-source threshold voltage as a function of junction temperature



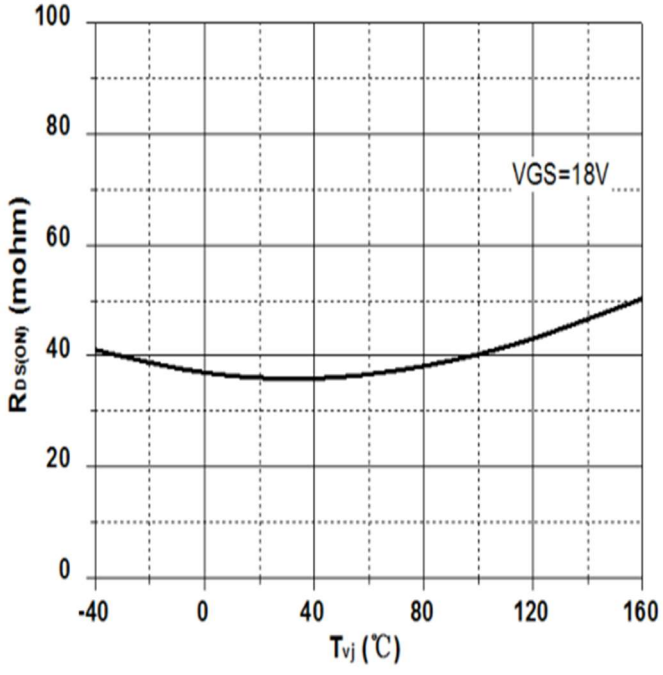
$V_{GS(th)}$=f(T_j); I_{DS}=5mA; V_{GS}=V_{DS}

Diagram 6: Typ. Capacitance as a function of drain-source voltage



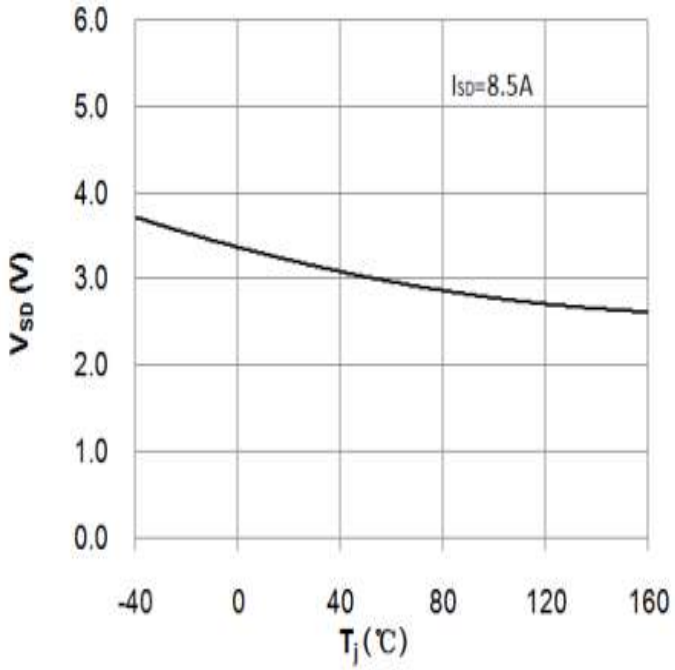
C=f(V_{DS});V_{GS}=0V; f=1MHz

Diagram 7: Typical on-resistance as a function of junction temperature



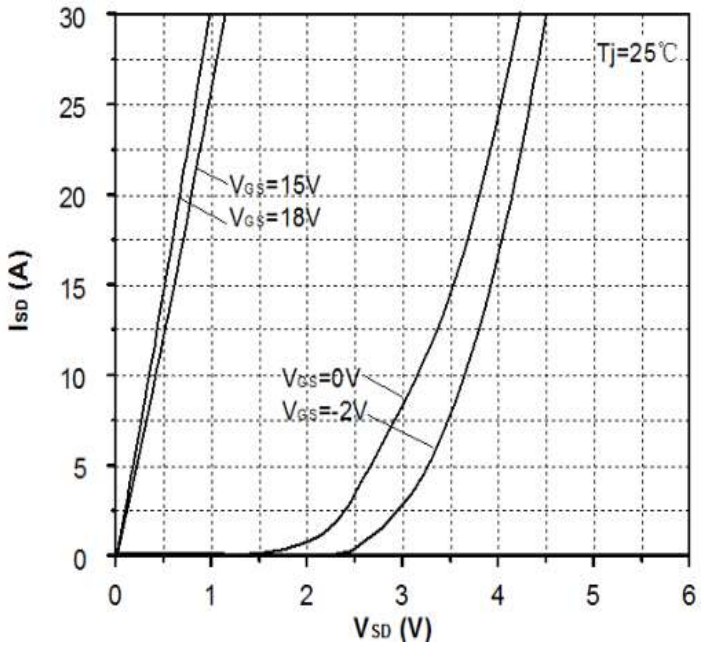
$R_{DS(ON)}$=f(T_j);I_{DS}=8.5A

Diagram 8: Typical body diodes forward voltage as function of junction temperature



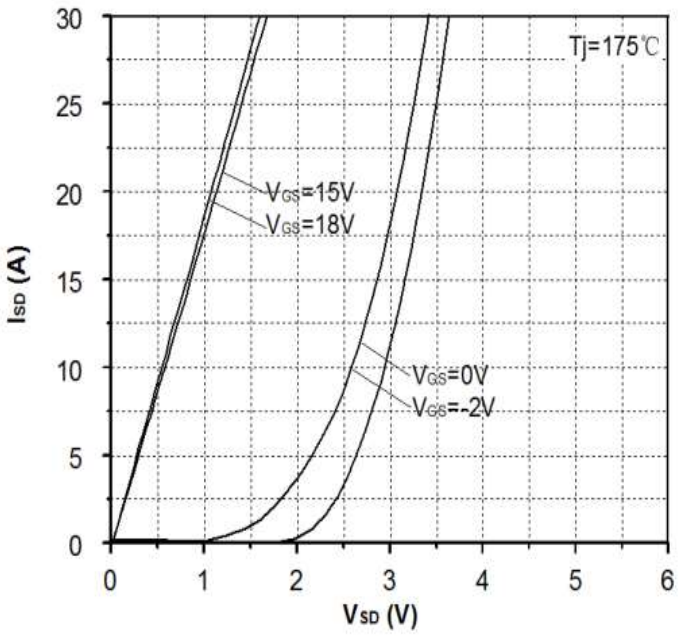
V_{SD}=f(T_j);V_{GS}=0V; I_{SD}=8.5A

Diagram 9: Typical body diodes forward current as function of forward voltage, V_{GS} as parameter



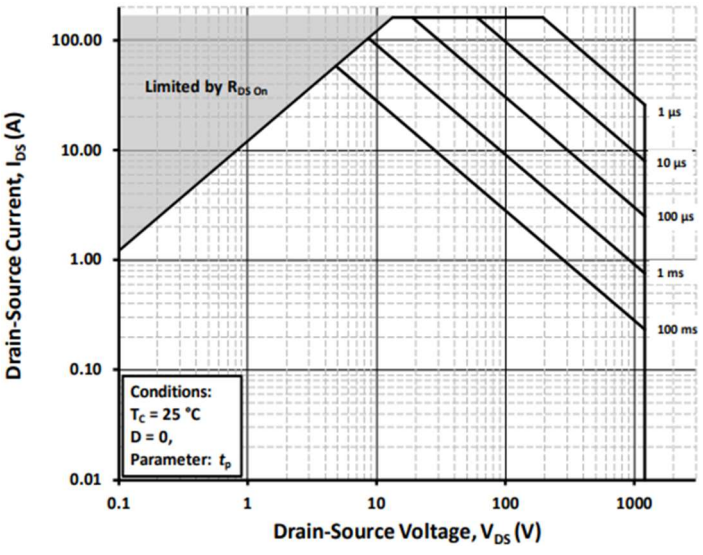
$I_{SD}=f(V_{SD})$; T_j=25 °C

Diagram 10: Typical body diodes forward current as function of forward voltage, V_{GS} as parameter



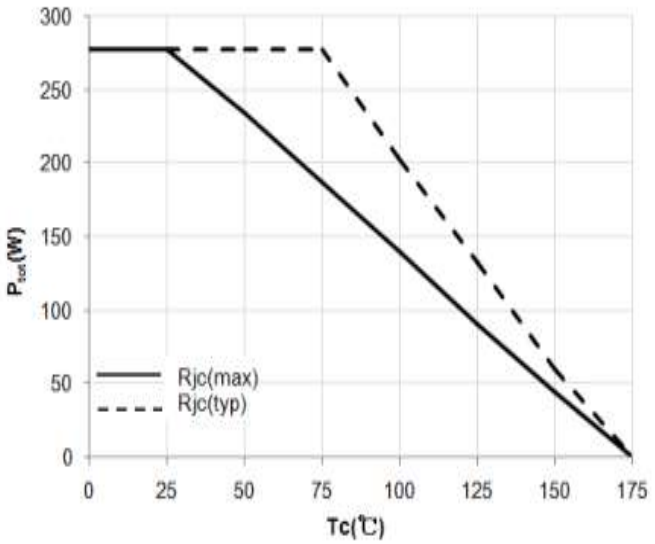
$I_{SD}=f(V_{SD})$; T_j=175 °C

Diagram 11: Safe operating area(SOA)



V_{GS}=0/18V; T_C=25 °C; T_j<175 °C

Diagram 12: Power dissipation as a function od case temperature limited by bond wire



P_{tot}= f(T_C)

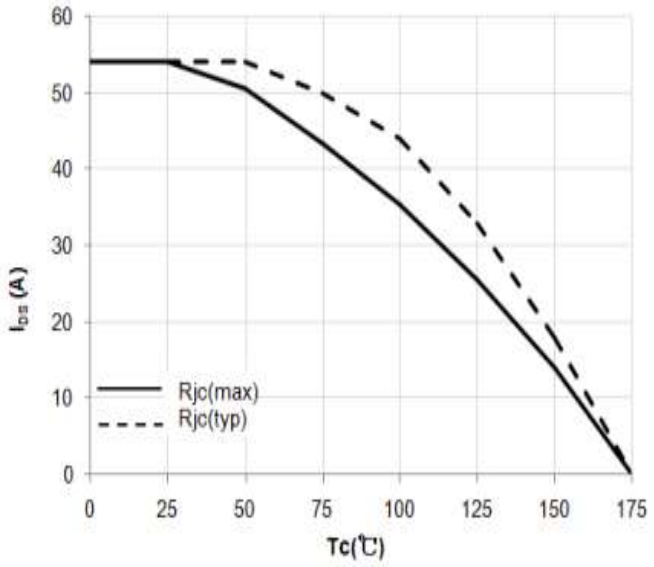
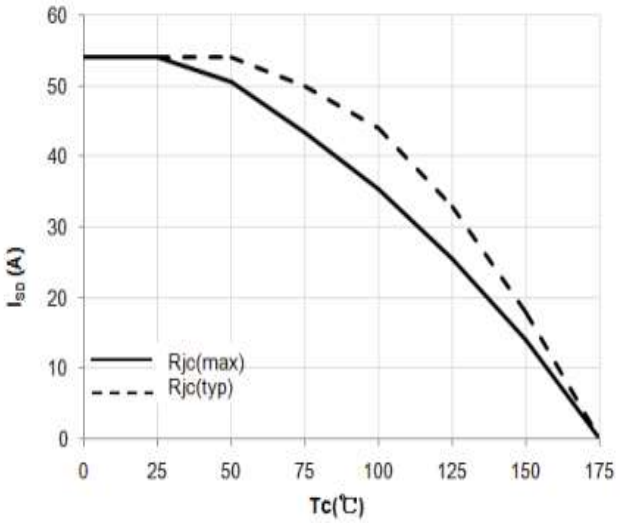
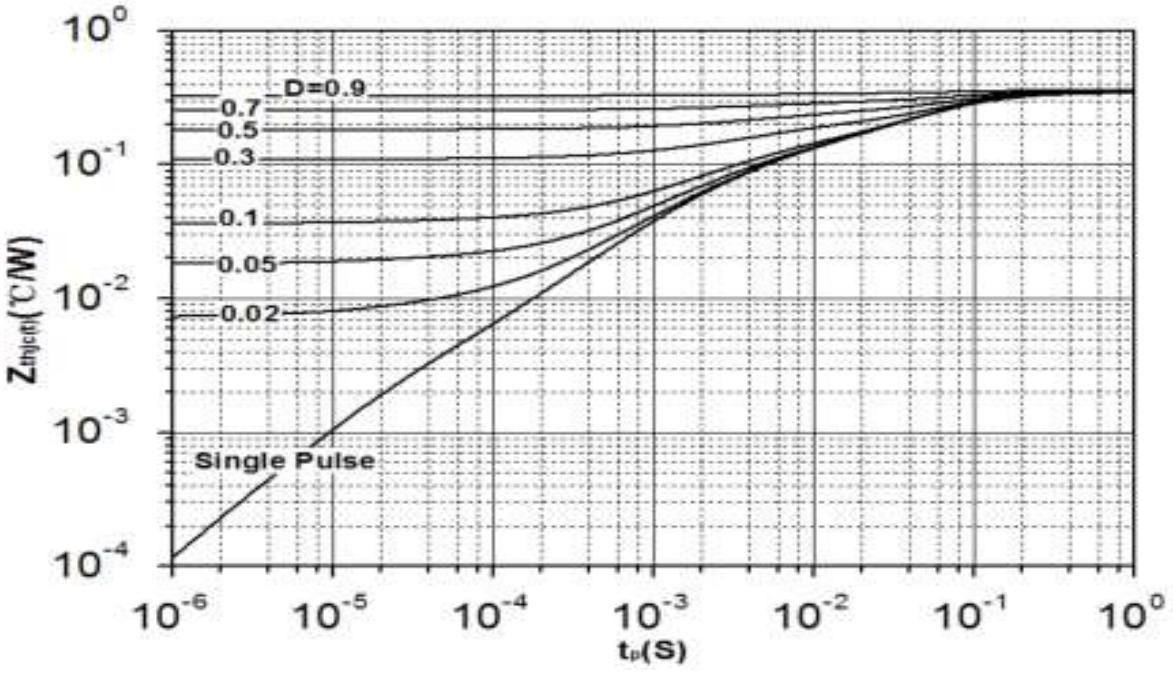
Diagram 13: Maximum DC drain to source current as a function of case temperature limited by bond wire	Diagram 14: Maximum source to drain current as a function of case temperature limited by bond wire
	
I_{DS}= f(T_C)	I_{SD}= f(T_C), V_{GS}=0V

Diagram 15: Max. transient thermal resistance(MOSFET/diodes)



$Z_{th(j\text{-}c,max)}$= f(t_p),parameter D= t_p/T

5 Test Circuits

Table 8 Diode characteristics

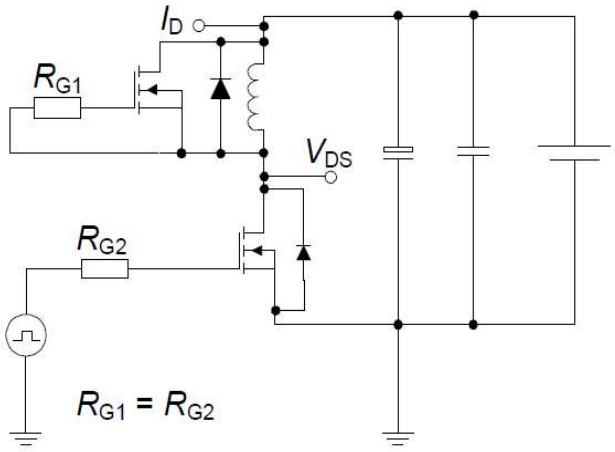
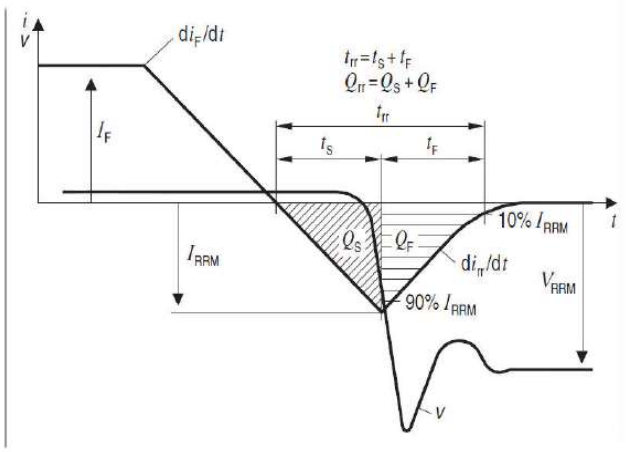
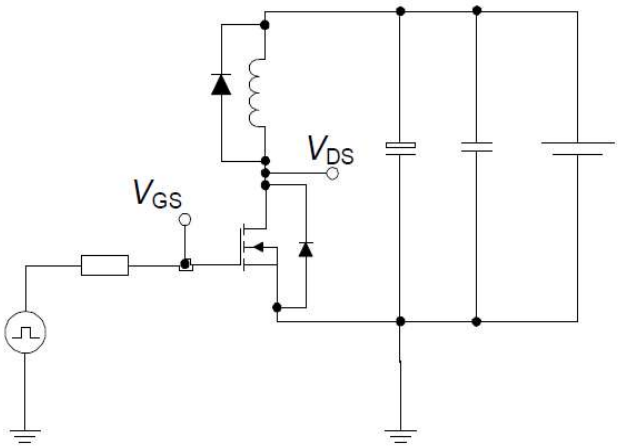
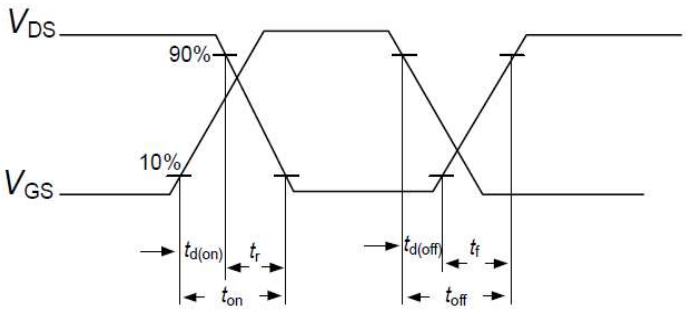
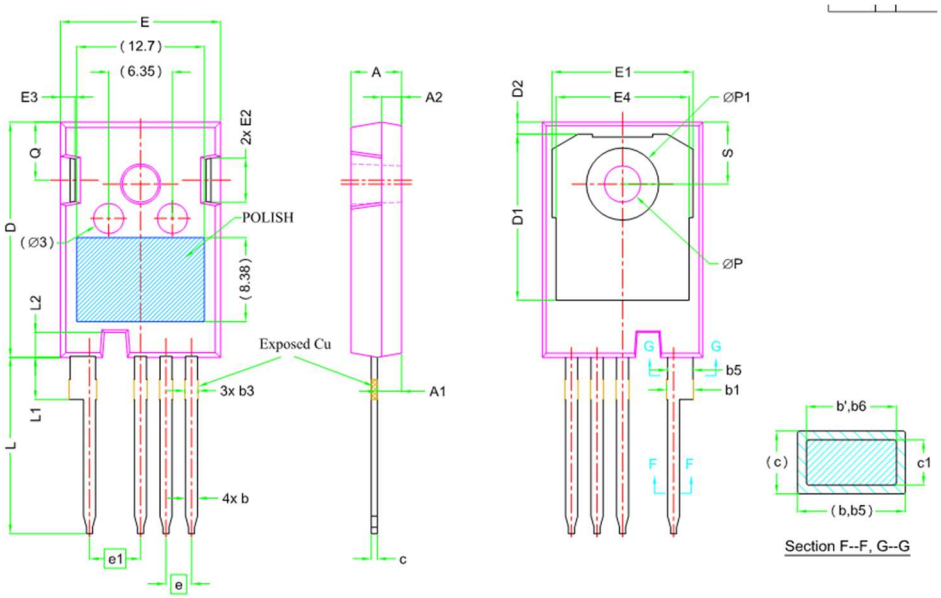
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

Switching times test circuit for inductive load	Switching times waveform
	

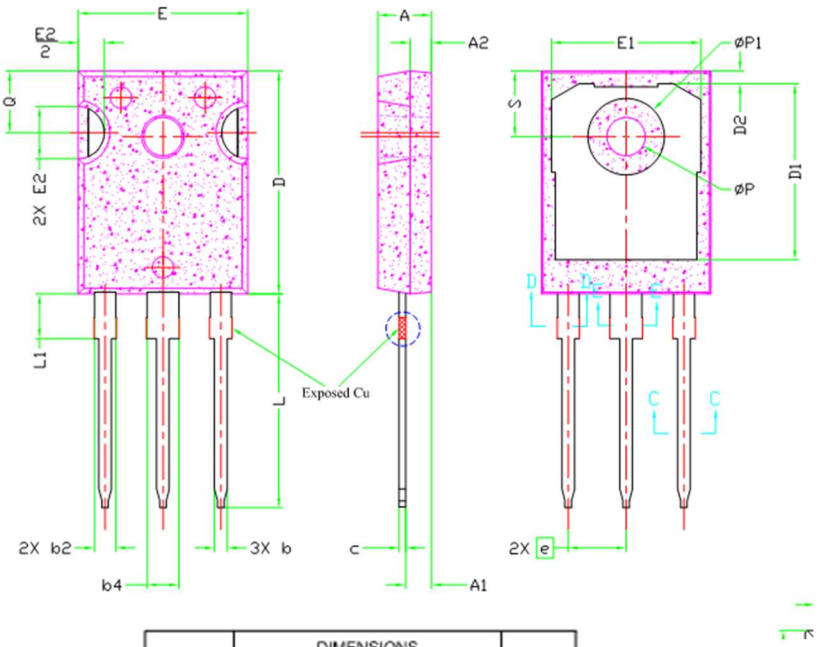
6 Package Outlines

TO-247-4L



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	4.83	5.02	5.21
A1	2.29	2.41	2.54
A2	1.91	2.00	2.16
b'	1.07	1.20	1.28
b	1.07	1.20	1.33
b1	2.39	2.67	2.94
b3	1.07	1.30	1.60
b5	2.39	2.53	2.69
b6	2.39	2.53	2.64
c	0.55	0.60	0.68
c1	0.55	0.60	0.65
D	23.30	23.45	23.60
D1	16.25	16.55	17.65
D2	0.95	1.19	1.25
E	15.75	15.94	16.13
E1	13.10	14.02	14.15
E2	3.68	4.40	5.10
E3	1.00	1.45	1.90
E4	12.38	13.26	13.43
e	2.54 BSC		
e1	5.08 BSC		
L	17.31	17.57	17.82
L1	3.97	4.19	4.37
L2	2.35	2.50	2.65
ØP	3.51	3.61	3.65
ØP1	7.19 REF.		
Q	5.49	5.79	6.00
S	6.04	6.17	6.30

TO-247-3L



SYMBOL	DIMENSIONS			NOTES
	MIN.	NOM.	MAX.	
A	4.83	5.02	5.21	
A1	2.29	2.41	2.55	
A2	1.50	2.00	2.49	
b	1.12	1.20	1.33	
b1	1.12	1.20	1.28	
b2	1.91	2.00	2.39	6
b3	1.91	2.00	2.34	
b4	2.87	3.00	3.22	6, 8
b5	2.87	3.00	3.18	
c	0.55	0.60	0.69	6
c1	0.55	0.60	0.65	
D	20.80	20.95	21.10	4
D1	16.25	16.55	17.65	5
D2	0.51	1.19	1.35	
E	15.75	15.94	16.13	4
E1	13.46	14.02	14.16	5
E2	4.32	4.91	5.49	3
e	5.44BSC			
L	19.81	20.07	20.32	
L1	4.10	4.19	4.40	6
øP	3.56	3.61	3.65	7
øP1	7.19REF.			
Q	5.39	5.79	6.20	
S	6.04	6.17	6.30	

Note:
1. Package Reference: JEDEC TO247, Variation AD.
2. All Dimensions Are In mm.
3. Slot Required, Notch May Be Rounded
4. Dimension D & E Do Not Include Mold Flash. Mold Flash Shall Not Exceed 0.127mm Pre Side. These Dimensions Are Measured At The Outermost Extreme Of The Plastic Body.
5. Thermal Pad Contour Optional Within Dimension D1 & E1.
6. Lead Finish Uncontrolled In L1.
7. ØP To Have A Maximum Draft Angle Of 1.5° To The Top Of The Part With A Maximum Hole Diameter Of 3.91mm.
8. Dimension "b2" And "b4" Does Not Include Dambar Protrusion. Allowable Dambar Protrusion Shall Be 0.10mm Total In Excess Of "b2" And "b4" Dimension At Maximum Material Condition.

Revision History

Revision	Date	Subjects (major changes since last revision)
1.1	2021-10-13	Preliminary version
1.2	2021-11-12	Update version
1.3	2022-02-07	Updated SOA diagram and Vth